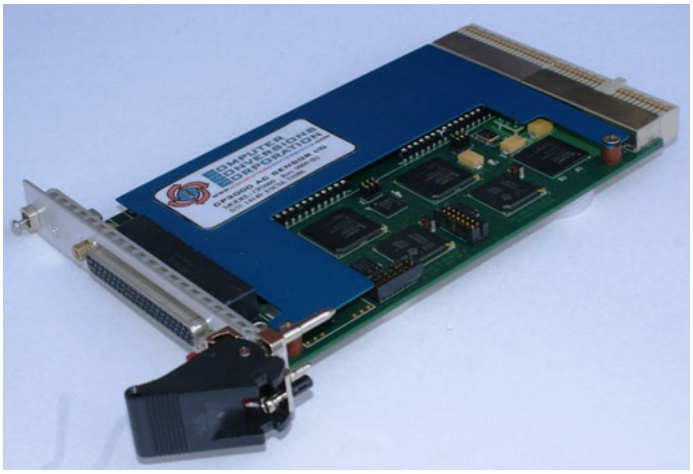
COMPUTER CONVERSIONS CORPORATION
www.computerconversions.com
6 Dunton Ct , E Northport, NY 11731 (631)261-3300 Fax. 261-3308

CP3000 SERIES

3U COMPACT PCI cPCI / PXI™ 4/8 SYNCHRO, RESOLVER & LVDT ISOLATED I/O CARD PLUS

FEATURES

- 4/8 synchro resolver LVDT input channels.
- Frequency: 47-10,000 Hz.
- Voltages: 115/90V. and universal 2-28VAC.
- Accuracy: ± 1 arc. minute.
- Digital Velocity to +/- 150 RPS.
- Programmable sensor select.
- 4 channels high power ultra-efficient on-board reference supplies.
- ± 10VDC linear DC analog outputs with programmable offsets (4/card)



Overview

The CP3000 Series are Single Slot 3U size Compact PCI **(cPCI)** compatable Synchro / Resolver input cards.

These cards are ideally suited for commercial, industrial and COTS military concerns using a rugged cPCI bus compatible computer in typical applications as dynamic pan and tilt camera stabilization, antenna and/or radar platforms and targetting applications that require a simple means of accurate stabilization in addition to mulltiple axis' of absolute position feedback for ancilliaries.

The cPCI-A74 provides up to 2 channels of dynamic Synchro or Resolver Control Transformer functions, plus up to

8 channels of Synchro or Resolver inputs,and an optional high efficiency programmable reference supply source for exciting various synchro/resolver sensors.

Optionally up to 4 channels of input with up to 4 auxillary reference supply sources is available.

Both industrial and COTS military grade (extended) temperature range versions are available.

100% Transformer Isolation is provided for all AC I/O, eliminating concerns for ground-loops, ground interjected (intermittent and ghostly) field noise, inductive surges,differing potentials, and high voltage field transients from effecting the card itself,the sensitive cPCI bus backplane and any other device or system sharing these signals.

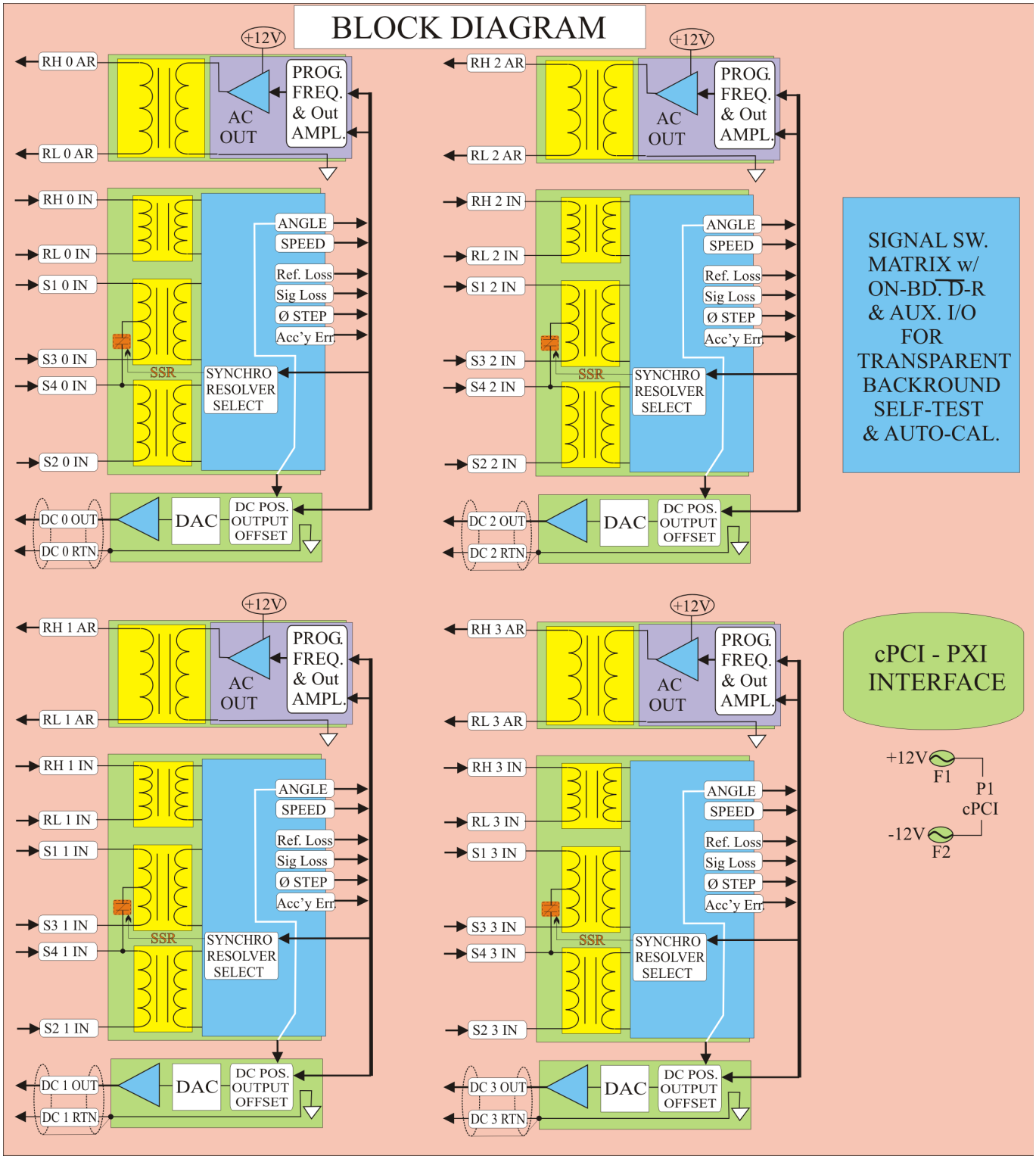
Independent Isolation is provided for each channel to eliminate any common returns or ground loops. Because there is no connection to ground or need for common connections or I/O circuit loops; the user has increased protection against lightning in that the field sensor I/O does not provide a ground reference of attraction.

The input channel Syncro / Resolver Input Channels are supplied with internal mirror I/O that is used toexcersize input circuitry functionality to provide continuous and comprehensive self testing that operates quietly in the backround without any user programming or intervention required.
The interface is a solidly-reliable / high-speed, true **32 bit "Long-Word-Level"** register access, inherent status report built-into every channel read, withut requiring additional interrupts or polling to report f fault indication and Built-in-Test that includes loss of signal, loss of reference, and loss of closed loop tracking report.

APPLICATIONS

- **UNMANNED GUIDED VEHICLES**
- **AIRCRAFT SENSOR TEST BEDS**
- **MOBILE TRACKING SYSTEMS**
- **NAVIGATION & DATA MULTIPLEXING**
- **NAVAL SYSTEMS**
- **RADAR & ANTENNA POSITIONING**
- **ROBOTICS**
- **ACTIVE PAN & TILT CONTROLS**
- **PLATFORM STABILIZATION SYSTEMS**

***PXI is a registered US trademark of PXI Systems Alliance.**



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Data Format Position Reads with embedded Fault Status

POSITION DATA READ

0 = Normal, 1 = card fault.

0 = Normal

0 = Normal, 1 = Loss of Reference Fault This Channel

0 = Normal, 1 = Loss of Signal Fault This Channel

0 = Normal, Tracking In-Range, 1 = Step Input Alert Detected *(Possible Fault,Channel Lagging)*

0 = Normal, 1 = Accuracy Error Fault This Channel *(Detected with Backround Testing)*

0 = Normal,

These 8 Bits
Fixed at Zero
(Not Used)

0	0	0	0	0	0	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

High Word = Status & Fault Report

Absolute Position Data
16 Bit Absolute Position Data
Binary Scaled Angle, MSB = 180°

0-65535 Representing 0 - 359.999°

UNSIGNED INTEGER LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Low Word = Position Data 16 Bits

cPCI CONFIGURATION SPACE HEADER				
31 16		15 0		
Device ID: 0001h		Vendor ID: 4CCCh		00h
Status		Command		04h
Class Code: FF 00 00h			Rev ID: 01h	08h
BIST	Header Type	Latency Timer	Cache Ln Size	0Ch
Base Address Register 0: FFFF FFF1h				10h
Base Address Register 1: FFF0 0008h				14h
Base Address Register 2				18h
Base Address Register 3				1Ch
Base Address Register 4				20h
Base Address Register 5				24h
Cardbus CIS Pointer				28h
Subsystem ID: 0001h		Subvendor ID: 4CCCh		2CH
Expansion ROM Base Address				30h
Reserved			Cap Ptr: 00h	34h
Reserved				38h
Max Lat: 00h	Min Gnt: 00h	Int Pin	Int Line	3Ch
Reserved				40h
				FCh
NOTES:				
1. Shaded address locations are not implemented.				
2. All unimplemented configuration space registers return a value of zero during configuration read cycles and no operation occurs during configuration write cycles.				
3. The cPCI interface does not handle burst configuration cycles and must disconnect. (Does handle Burst Read/Write Data)				

PIN TERMINATIONS:MODELS UP TO 8 CHANNELS INPUT WITH 1 AUX REFERENCE OUTPUT

SYNCHRO, RESOLVER & LVDT INPUT CHANNELS

PANEL J3 PINS	SIGNAL INPUT TYPE	BACK PLANE J2 PINS	S-D/R-D CHAN'L	PAIR IF MULTI
24	SD0-IN-S1	D20	0	CHAN 0 (FINE)
25	SD0-IN-S3	E20		
45	SD0-IN-S2	E21		
46	SD0-IN-S4	D21		
3	SD0-IN-RH	E19		
4	SD0-IN-RL	D19		
26	SD1-IN-S1	D17	1	PAIR IF MULTI W/ CHAN 1 (COARSE)
27	SD1-IN-S3	E17		
47	SD1-IN-S2	E18		
48	SD1-IN-S4	D18		
5	SD1-IN-RH	C19		
6	SD1-IN-RL	B19		
28	SD2-IN-S1	D15	2	CHAN 2 (FINE)
29	SD2-IN-S3	E15		
49	SD2-IN-S2	E16		
50	SD2-IN-S4	D16		
7	SD2-IN-RH	E14		
8	SD2-IN-RL	D14		
30	SD3-IN-S1	D12	3	PAIR IF MULTI W/ CHAN 3 (COARSE)
31	SD3-IN-S3	E12		
51	SD3-IN-S2	E13		
52	SD3-IN-S4	D13		
9	SD3-IN-RH	C14		
10	SD3-IN-RL	B14		
32	SD4-IN-S1	D2	4	CHAN 4 (FINE)
33	SD4-IN-S3	E2		
53	SD4-IN-S2	E3		
54	SD4-IN-S4	D3		
11	SD4-IN-RH	E4		
12	SD4-IN-RL	D4		
34	SD5-IN-S1	D5	5	PAIR IF MULTI W/ CHAN 5 (COARSE)
35	SD5-IN-S3	E5		
55	SD5-IN-S2	E6		
56	SD5-IN-S4	D6		
13	SD5-IN-RH	C4		
14	SD5-IN-RL	B4		

SYNCHRO, RESOLVER & LVDT INPUT CHANNELS (CONT'D)

PANEL J3 PINS	SIGNAL INPUT TYPE	BACK PLANE J2 PINS	S-D/R-D CHAN'L	PAIR IF MULTI
36	SD6-IN-S1	D7	6	CHAN 6 (FINE)
37	SD6-IN-S3	E7		
57	SD6-IN-S2	E8		
58	SD6-IN-S4	D8		
15	SD6-IN-RH	E9		
16	SD6-IN-RL	D9		
38	SD7-IN-S1	D10	7	PAIR IF MULTI W/ CHAN 7 (COARSE)
39	SD7-IN-S3	E10		
59	SD7-IN-S2	E11		
60	SD7-IN-S4	D11		
17	SD7-IN-RH	C9		
18	SD7-IN-RL	B9		
61	SDN-IN-LH1	-	ANY	EXTERNAL LATCH INPUT
62	SDN-IN-LLO	-		
1	AR0-OUT-RH	E1	A (ANY)	PROGRAMMABLE REFERENCE SUPPLY
22		-		
23	AR0-OUT-RL	D1		
43		-		
20	+12V EXT.-IN	NOT REQ'D	IF USED-REMOVE (F1)	
21				
2	GND	B1		
44		-		
41	-	DO NOT USE		
42	-			

J2 = TYCO/AMP # 188836-1 (110 PIN 2MM HM RCPT, UN-SHIELDED)
OR
J2 = TYCO/AMP # 5352152-1 (110 PIN 2MM HM RCPT, SHIELDED)

J3 = TYCO/AMP # 748394-5 (62 PIN "D" RCPT)

ADDITIONAL NOTES:
1) * DC OUTPUT GROUNDS, USE ONLY 1 PER DESTINATION.
2) J2 OPTIONAL

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PIN TERMINATIONS: MODELS UP TO 4 CHANNELS INPUT WITH UP TO 4 REFERENCE OUTPUTS

SYNCHRO, RESOLVER & LVDT INPUT CHANNELS

PANEL J3 PINS	SIGNAL INPUT TYPE	BACK PLANE J2 PINS	S-D/R-D CHAN'L	PAIR IF MULTI
36	SD0-OUT-DC	D7		± 10VDC OUTPUT **
37	SD0-OUT-GND*	E7		
24	SD0-IN-S1	D20	0	CHAN 0 (FINE) PAIR IF MULTI CHAN 1 (COARSE)
25	SD0-IN-S3	E20		
45	SD0-IN-S2	E21		
46	SD0-IN-S4	D21		
3	SD0-IN-RH	E19		
4	SD0-IN-RL	D19		
26	SD1-IN-S1	D17	1	
27	SD1-IN-S3	E17		
47	SD1-IN-S2	E18		
48	SD1-IN-S4	D18		
5	SD1-IN-RH	C19		
6	SD1-IN-RL	B19		
57	SD1-OUT-DC	E8		± 10VDC OUTPUT **
58	SD1-OUT-GND*	D8		
38	SD2-OUT-DC	D10		± 10VDC OUTPUT **
39	SD2-OUT-GND*	E10		
28	SD2-IN-S1	D15	2	CHAN 2 (FINE) PAIR IF MULTI CHAN 3 (COARSE)
29	SD2-IN-S3	E15		
49	SD2-IN-S2	E16		
50	SD2-IN-S4	D16		
7	SD2-IN-RH	E14		
8	SD2-IN-RL	D14		
30	SD3-IN-S1	D12	3	
31	SD3-IN-S3	E12		
51	SD3-IN-S2	E13		
52	SD3-IN-S4	D13		
9	SD3-IN-RH	C14		
10	SD3-IN-RL	B14		
59	SD3-OUT-DC	E11		± 10VDC OUTPUT**
60	SD3-OUT-GND*	D11		
61	SDN-IN-LH1	-	ANY	EXTERNAL LATCH INPUT (optional)
62	SDN-IN-LLO	-		

SYNCHRO, RESOLVER & LVDT INPUT CHANNELS (CONT'D)

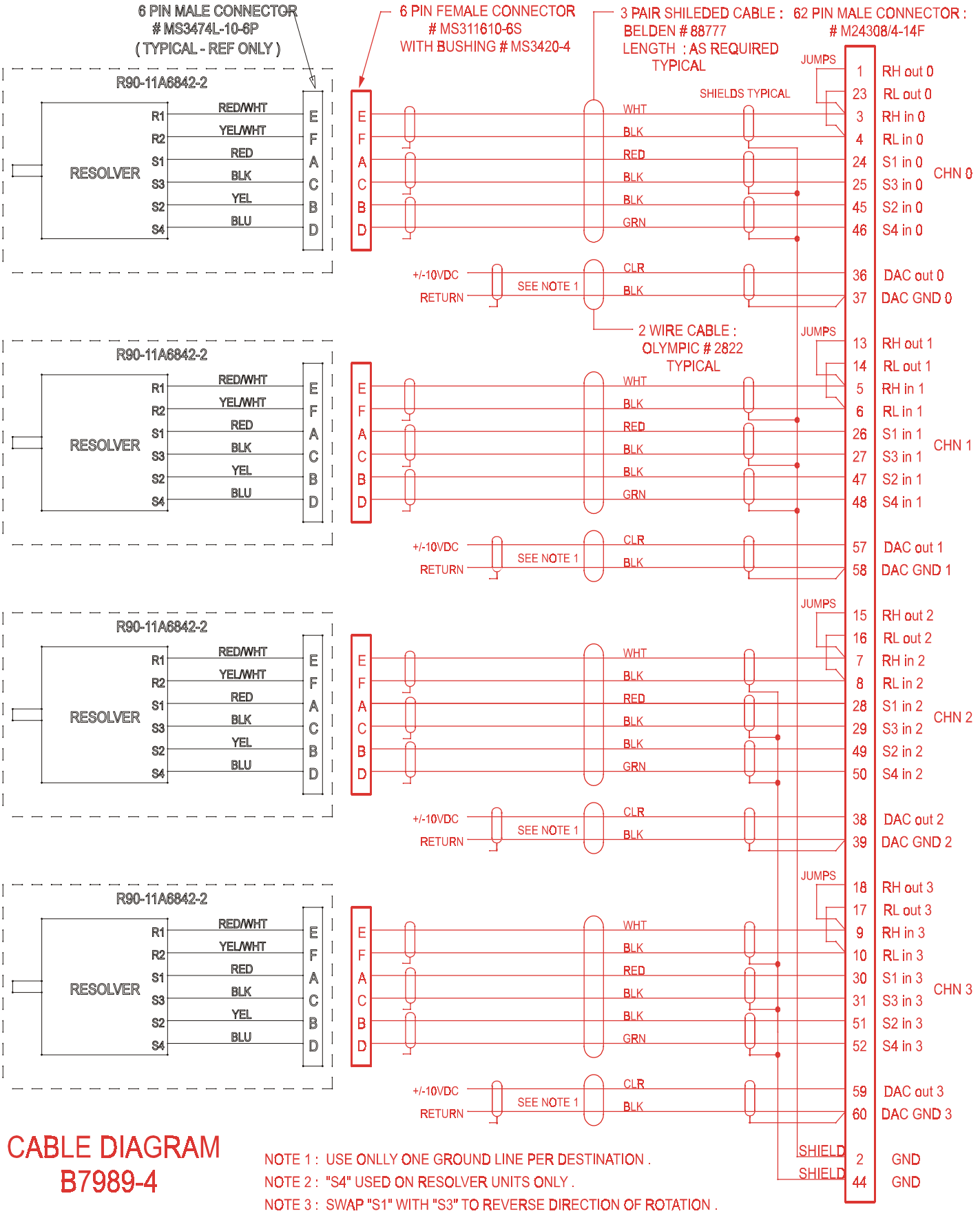
PANEL J3 PINS	SIGNAL INPUT TYPE	BACK PLANE J2 PINS	S-D/R-D CHAN'L	PAIR IF MULTI
1	AR0-OUT-RH	E1	A (ANY)	PROGRAMMABLE REFERENCE SUPPLY A
23	AR0-OUT-RL	D1		
13	AR1-OUT-RH	C4	B (ANY)	PROGRAMMABLE REFERENCE SUPPLY B
14	AR1-OUT-RL	B4		
15	AR2-OUT-RH	E9	C (ANY)	PROGRAMMABLE REFERENCE SUPPLY C
16	AR2-OUT-RL	D9		
18	AR3-OUT-RH	B9	D (ANY)	PROGRAMMABLE REFERENCE SUPPLY D
17	AR3-OUT-RL	C9		
20 21	+12V EXT.-IN	NOT REQ'D	IF USED-REMOVE (F1)	
2 44	GND	B1 -		
41	-	DO NOT USE		
42	-			

J2 = TYCO/AMP # 188836-1 (110 PIN 2MM HM RCPT, UN-SHIELDED)
OR
J2 = TYCO/AMP # 5352152-1 (110 PIN 2MM HM RCPT, SHIELDE D)

J3 = TYCO/AMP # 748394-5 (62 PIN "D" RCPT)

ADDITIONAL NOTES:
1) * DC OUTPUT GROUNDS, USE ONLY 1 PER DESTINATION.
2) J2 OPTIONAL
** DC ANALOG OUTPUT OPTIONAL.

ADDRESS MAP			
BASE +	**FUNCTION**	**CHANNEL**	**R/W**
000 h	**POSITION** READ W/STATUS	0	R
004 h		1	R
008 h		2	R
00C h		3	R
010 h		4	R
014 h		5	R
018 h		6	R
01C h		7	R
020 h	**W/STATUS**	0	R
024 h		1	R
028 h		2	R
02C h		3	R
030 h		4	R
034 h		5	R
038 h		6	R
03C h		7	R
060 h	**SET ANALOG** OUTPUT OFFSET	0	W/R
064 h		1	W/R
068 h		2	W/R
06C h		3	W/R
0A0 h	**SET ACTIVE** CHANNELS	ALL	W/R
0A4 h	**SET LATCH EN.**	ALL	W/R
02A h	**SET SENSOR TYPE** SYNCHRO 2 WIRE LVDT or 3 WIRE LVDT	ALL	W/R
120 h	**SET FREQUENCY**	AUX 0	W/R
124 h	**SET VOLTS**	AUX 0	W/R
128 h	**SET FREQUENCY**	AUX 1	W/R
12C h	**SET VOLTS**	AUX 1	W/R
130 h	**SET FREQUENCY**	AUX 2	W/R
134 h	**SET VOLTS**	AUX 2	W/R
138 h	**SET FREQUENCY**	AUX 3	W/R
13C h	**SET VOLTS**	AUX 3	W/R



CABLE DIAGRAM
B7989-4

NOTE 1 : USE ONLLY ONE GROUND LINE PER DESTINATION .
NOTE 2 : "S4" USED ON RESOLVER UNITS ONLY .
NOTE 3 : SWAP "S1" WITH "S3" TO REVERSE DIRECTION OF ROTATION .

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