Power Amplifier Envelope Tracking and Digital Pre-distortion/Crest Factor Reduction Technologies and PXIe Solution





#### **Robert Hood** Solutions Business Development



### Agenda

### PA ET/DPD/CFR Test Technologies

- What are the key challenges for PA design?
- What are the CFR, DPD and ET technologies for PA?

#### **Keysight PA Test Reference Solution**

- PXIe Solution for PA Test
- PXIe Solution Architecture



# The Evolution of a Handset PA



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## ET and PADs inside The iPhone 6

Orange: Qualcomm MDM 9625M LTE Modem Yellow: Skyworks 77802-23 Low band LTE PAD Green: Avago A8020 High band PAD Blue: Avago A8010 Ultra high band PAD + FBARs Purple: Skyworks 77803-20 Mid band LTE PAD Black IvenSense MP67B 6 axis gyro / accelerometer

iPhone 6 teardown iFixit Sept 2014





Red: Qualcomm QFE1000 ETPS Orange RFMD RF5159 Antenna switch Yellow Skyworks 77356-8 Mid Band PAD other side of PCA



Black: Qualcomm WTR1625L RF transceiver Red: Qualcomm WFR1620 Rx only companion, for carrier aggregation Orange: Qualcomm PM8109 Power management IC



# Three Methods to increase PA efficiency and linearity



# **ET: Envelope Tracking**



### **DPD: Digital Pre-Distortion**



### **CFR: Crest Factor Reduction**



RF PA/FEM I Reference Solution

# Envelope Tracking vs. Fixed Supply - Concept





# Envelope Tracking - The How & Why



Continuously adjust the supply voltage to change the PA's operating point

- Improve battery life
- Increase RF amplifier performance over broad frequencies
- Lower distortion
- Reduce heat dissipation



# **Envelop Tracking - Shaping Table Design**



- A linear relationship between the IQ magnitude & modulated supply is not optimum
- A shaping table is used to optimize the PA's performance for efficiency or linearity



# Digital Pre-Distortion (DPD) - Concept



DPD corrects PA nonlinearities resulting in higher performing power amplifiers



# What is the DPD test procedure?



# Crest Factor Reduction - The How & Why

# Reduce the PAPR to limit distortion produced in the PA $V_{Out}$



- CFR is not a linearization technique
- Two methods widely used: 1) Clipping and Filtering 2) Peak Windowing



# CFR – Peak Windowing

- Peak windowing aims to smooth the sharp corners which result from hard clipping
- In the peak windowing algorithm, clipping is implemented by multiplying the original signal in the region of the peak with a windowing function such as Kaiser, Gaussian and Hamming.





# ACP-EVM Performance Trade-off Using CFR

Example: CFR using clipping & filtering

If ACPR fails the 3GPP spec., applying CFR can give a few dB improvement, enough to pass or provide some margin but EVM will increase.





# Where do ET, DPD and CFR apply?

	ET	DPD	CFR
WLAN	Exploring/Verification On/Off HS (Mainly in R&D)	Access Point (AP) and Station (STA)	Access Point (AP) and Station (STA)
Cellular	UE	BTS (normally complicated with real-time feedback) UE (normally pen-loop)	BTS
Benefit	Save Power Improve linearity	Improve Linearity	Improve linearity (PAPR)



### Techniques to Mitigate PAPR Related Issues Know your alphabet

#### Amplifier sizing

#### Back-off

#### **Crest Factor Reduction**

- Distort RF PA input signal to reduce distortion produced by PA compression
- Choose the method and compression level to match the PA characteristics

#### **Digital pre-distortion**

- Distort the RF PA input to cancel distortion produced by the PA
- Choose the method to suit the baseband capability and the PA characteristics

#### Envelope tracking

- Drive the RF PA with a fully modulated RF signal and synchronously modulate the PA supply voltage
- Adjust the RF PA operating point by controlling the RF / Envelope magnitude ratio, called the shaping table, or de-troughing function



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# What do we need to test in a PA?

#### Basic Performance

- P<sub>out MAX</sub>, P<sub>3dB</sub>
  - With ramped power signal
- Gain, ACPR, PAE
  - With power servo technique
- Good Neighbor
  - Harmonic generation, intermod, spectral regrowth, in-band Rx noise
- Compatibility
  - Return loss, AM/AM, AM/PM, EVM, mismatch tolerance
    - Passive components of PAD filters, duplexers
- Measurements as a function of frequency and output power level
- Performance under ET and DPD?





### Keysight Reference Solution Typical Block Diagram (Release3.0: VSG/VSA)



## Keysight Reference Solution Typ. Block Diagram (Releases3.1: VXT)



# Power Amplifier Reference Solution

### Minimize Customer Investment to Evaluate & Deploy

- Keysight Provided "Recipe" for Power Amplifier Tests using Keysight PXI Modules with LXI and Third Party Products, as needed
- Provides Demonstration of Capabilities, Measurement Ranges and Test Times
- Configurable to Test Customer Devices without Code Changes for First Level Evaluation
- Source Code to Minimize Porting Instruments into Customer's Test Environment for Detailed Evaluation and Deployment
- Focus on PA design/validation/test and production test including support for ET and DPD
- The bottom line…
  - Evaluate quicker, leverage Keysight's measurement knowledge, deploy with lower risk



# **Evaluation Software Environment**





### **RF PA/FEM Characterization & Test Reference Solution** ET/ DPD Evaluation Software Environment



### **RF PA/FEM Characterization & Test Reference Solution** Optimized for insight – Code Example

- • • ×

Init

Local VSA

VSA/G DC/R	FE S Parameters LTE	s WLAN
📃 Enabl	e ET	
Use Use	DPD Wavefroms for All LT	TE Tests
N7614B DPD	/ET Settings	N7C14P Halo
Waveform/C	CFR/ET DPD	
-DPD Mo	del	_
🔽 Enab	le DPD	Waveform Length 0.5 🚖 ms
Model Ty	pe Look-up Table	→ Analysis Duration 200.0 → uS
Iterations	s 1 🚔	Analysis Delay 2.6 🤿 uS
LUT Pa	rameters	Memory/Voltera Parameters
LUT Siz	128 🌩	Model ID 👻
AM/AM	Polynomial 3 🚔	Memory Order 1
AM/PM	Polynomial 3 🚔	Nonlinear Order 5
		Cross Term Order 5
		Odd Orders Only
		eset To Open Data View Users

#### Extract LUT Values and Memory Model Polynomial Coefficients





# FPGA Speed Enhancement Architecture



## Some measurement speed improvements \*

For ET/DPD capable UE 4G Power Amp

		Host PC Based			M9451A FPGA-base	<u>ed</u>
<u>Waveform</u>	Model Extract	<u>Model Apply</u>	Total Test Time	Model Extract	Model Apply	Total Test Time
5 MHz LTE	447.48 msec	45.78 ms	564.44 ms	4.04 ms	16.0 ms	69.52 ms
20 MHz LTE	1752.28 ms	169.92.5 ms	2101.14 ms	6.0 ms	63.0 ms	142.74 ms
						-

- M9037A embedded controller, M9381A VSG, M9393A VSA, H3353 AWG, M9451A FPGA
- 500 msec LTE waveform using ET and DPD
- Measurements made using power servo technique: Gain, PAE, ACPR, Delta EVM, 2<sup>nd</sup> through 6th harmonics
- All times averaged over 50 measurements



# Summary of Key Points

### Keysight's PXI Reference Solution for Power Amplifier Testing

- 1. Proven solution in DVT and manufacturing by top tier PA vendors.
- 2. Enables software reuse for <u>your</u> solution that reduces deployment effort, time and cost.
- 3. Provides support for emerging UE technologies including ET, DPD and uplink CA.
  - Market leading measurement precision and performance



# **Questions/Discussion**





# M9381A VSG

- Performance characteristics
- Frequency coverage from 1 MHz to 3 GHz or 6 GHz
- 10 µs switching speed with fast-tune, an exclusive baseband tuning technology innovation
- RF modulation bandwidth up to 160 MHz (± 0.3 to 0.5 dB flatness)
- ± 0.15 to 1.0 dB absolute amplitude accuracy
- Software Enhancements in 1.2 release:
- Shared Frequency Reference
- PXI backplane triggers
- New PLL Mode (Best Wide Offset) for WLAN EVM and GSM/EDGE ORFS optimization
- Improved sync out trigger for Envelope Tracking
- Software Enhancements in 1.3 release:
- Add Time Synchronous MIMO capability, channel-to-channel deviation <20 ns</li>





### **Meet the M9393A PXIe Performance VSA** The world's fastest, most accurate µW PXI VSA



- Leverages proven designs
  - Downconverter derived from PXA
  - FieldFox calibrator for excellent accuracy
  - M9391A PXI VSA digitizer & reference modules



- Deploys cutting-edge technology
  - Novel solid-state switches for speed & reliability Unique Keysight Labs production process to lower size & cost

Frequency range	9 kHz to 8.4/ 14/ 18/ 27 GHz
Analysis BW	40/100/160 MHz
Amplitude accy	+/15 dB
Tuning speed	150 us
Size	5 slots (4 + ref)





# Keysight M9420A VXT Vector Transceiver Compress Time, Compress Test

And/or





Create custom PXI solution

Description	Performance	
Frequency range	60MHz to 3.8GHz or 6GHz	
Analysis bandwidth	40MHz, 80MHz or 160MHz	
Output Power	Standard: +10 dBm Optional: +18 dBm	
Memory depth	256 MSa or 512 Msa	
Slot Width	4-slots width (+ reference module)	
4 RF Ports	Tx, Rx, Full Duplex, Half Duplex	

#### HW Accelerated speed with high density & accuracy

- Combined VSG and VSA in single, 4-slot PXIe module
- FPGA-Accelerated speed with high density & accuracy
- Trusted X-Series software: industry tested algorithms, with code compatibility & bench top usability
- Ease evaluation and programming with ready-to-use IVI drivers, SCPI commands and integration with the Keysight PA Reference Solution

### Create a flexible modular solution with one PXIe mainframe



# Ready to Run for Single Antenna Test **Optional Full & Half Duplex Ports**

RF output port: Pure source output port provides highest output power level

RF Half Duplex port: Internally switched RF input or output port

RF Full Duplex port: Bi-directional communication

**RF input port**: Pure receiver input port provide best DANL performance.



#### Bi-directional & switched communication over single port connection.



Typical transceiver configuration



#### AOU-H3300/H3400 Series – Block Diagram





- F-Models (AOU-H3300F/H3400F) allow hardware implementation of custom FPGA algorithms
  - Output equalization / Digital pre-distortion
  - Custom filtering
  - Real-time waveform calculation/generation

RF PA/FEM Reference Solution

# M9451A Measurement Acceleration Module

- Dedicated FPGA module
- Initial release of gateware supports ET/DPD measurement acceleration only
- Module can be added to Keysight VSA/G PXI system for PA test
- APIs provided for integration into the customer test environment
- Uses same Keysight DPD methods utilized in SystemVue and N7614B PA test software
- Gateware Release 1.1 (Aug 2015)
  - Minor update; add Memory Polynomial method support
- Gateware Release 1.2 (end 2015)
  - Enable customized DPD methods
- Release 2.0 open programming (2016)
  - Ability for users to develop and embed own IP into the FPGA





## PXIe Vector Network Analyzer, M937XA

Driving down the size of test

- Full two-port network analyzer in just one slot
- Widest available frequency range:
  300 kHz to 4, 6.5, 9, 14, 20, 26.5 GHz
- Best PXI VNA performance in four key areas:
  - Speed: 18 msec across 401 points
  - Dynamic range: 114 dB (9 GHz), 110 dB (20 GHz)
  - Trace noise: < 0.003 dB specified,</li>
     < 0.001 dB typical</li>
  - Stability: ±0.005 dB/°C at 4 GHz, ±0.020 dB/°C at 26.5 GHz





# M9195A Digital Stimulus Response (DSR) Product Overview – Key Features for DUT RFFE Control

#### Digital I/O

- 16 bidirectional channels
  - ✓ Programmable logic levels: -1.5V to +6.5V (±75mA)
  - ✓ 125M vectors/ch memory
  - ✓ Up to 250 MHz pattern rate (with RZ support)
  - ✓ I/O channels are also capable of PPMU and static digital
- 4 high voltage IO channels for flash memory programming
- 4 open drain ports for fixture control

#### Vector Timing

- Independent channels: per channel & per clock cycle IO control, per vector timing, per period timing, on-the-fly modification
- <u>1 nsec</u>edge placement resolution for per period vector control
- Per channel programmable stimulus/response compensation delay: up to 250ns with 50ps resolution
- STIL programming support







# ET Standards & Industry Groups

MIPI eTrak mipi alliance

- Specification for an analog interface between BBIC/RF IC and envelope tracking power supply (ETPS)
- Keysight (Agilent) is MIPI member, and a contributor to the group



- Advocates the benefits of ET
- Standardize interface and system specifications



