Hardware Specification

PCI eXtensions for Instrumentation

An Implementation of **CompactPCI®**

Revision 2.2
September 22, 2004

IMPORTANT INFORMATION

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PXI Specification Revision History

This section is an overview of the revision history of the PXI specification.

Revision 1.0, August 20, 1997

This is the first public revision of the PXI specification.

Revision 2.0, July 28, 2000

This revision incorporates changes that include but are not limited to the following:

- Transfer of the specification ownership to the PXI System Alliance.
- Modification of pin assignment to comply with PICMG 2.0 R3.0 that include addition of GA0-GA4 signals to all slots, removal of PRST#, DEG#, and FAL# from peripheral slots, addition of IPMB bus to all slots, addition of HEALTHY# to all slots, addition of SMB bus to system slot, addition of BD_SEL# to peripheral slots, changing SYSEN# to UNC on peripheral slots, and changing IDSEL to GND on system slot.
- Removal of references to Serialized IRQ due to PICMG 2.0 R3.0 adoption.
- Addition of 66MHz PCI operation.
- Removal of J5 as a reserved connector.
- Allowance of J5 to be populated only in custom PXI boards and backplanes that are offered as a system.
- Allowance for star trigger routings other than only peripheral slots in first two segments in PXI backplanes with more than two segments.
- Allowance for the local bus to be routed between segments.
- Addition of rules about connecting the IDSEL lines of first segment PCI devices, bridges, and peripheral slots to AD[25:31] and routing peripheral slot INT lines to system slot INT lines based on the peripheral slot IDSEL to AD[25:31] connection.
- Increased required current on 3.3V for a 5V backplane to comply with requirement of 3.3V being available according to PICMG 2.0 R3.0
- Addition of Windows 98 and Windows 2000 software frameworks.
- Removal of requirements for PC 9X compliance for controllers and peripherals.
- Addition of segment divider glyph.
- Removal of SHALL NOT rule for chassis ground to digital ground connection and addition of SHOULD NOT recommendation for chassis ground to digital ground.
- Modification of requirements for EMC that includes changing IEC 61326-1:1997 to IEC 61326?1:1998 and IEC CISPR-11 to EN5501.
- Addition of maximum Voh and minimum Vol values for trigger bus.
- Modification of the legal notice.
- Addition of license requirement for use of the PXI logo.

Revision 2.1, February 4, 2003

This revision incorporates changes that include but are not limited to the following:

- Removal of software related rules (Refer to the now separate PXI Software Specification).
- Removal of J4 as a reserved connector.
- Addition of rules associated with 6U chassis that support stacking of two 3U modules in a single 6U slot.
- Addition of a rule that limits the maximum number of slots in a chassis to 31.
- Combining the chassis power supply minimum power requirements tables into one table and removing the recommended current entries in favor of required current entries.

- Increasing the -12V required current.
- Addition of the minimum current-handling requirement for each slot.
- Turning the recommendation that modules document their required current into a rule.
- Addition of a recommendation to limit the maximum power that a module dissipates within a chassis.
- Addition of a rule that requires filler panels to be installed in chassis slots that are not populated.
- Addition of an implementation note that recommends not mapping a module's registers mapped to PCI I/O Space.
- Modification of J2/P2 B19 and J2/P2 B21 pin assignments from GND to RSV on star trigger and peripheral pinouts.

Revision 2.2, September 22, 2004

This revision incorporates changes that include but are not limited to the following:

- Addition of a chassis class that does not support 64-bit PCI and allowance of controllers used in such a chassis to implement rear I/O.
- Addition of a low power chassis class that reduces the minimum power requirements.
- Addition of module grounding recommendations
- Addition of rules for 5V tolerance for PXI_CLK10 and PXI_CLK10_IN
- Addition of pull-up resistor requirements for the PXI_CLK10_IN signal.
- Addition of recommendation not to use low cost PLLs for PXI_CLK10 distribution
- Addition of an observation on circuit operation for transitioning between clock sources.
- Addition of a recommendation for modules using triggers to connect to all 8 triggers
- Addition of a rule that the pull-up on the PXI_STAR line be 20K Ohm or greater.
- Addition of a rule that puts requirements on the disabling of external 10 MHz clock sources.

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1. Introduction

This section describes the primary objectives and scope of the PCI eXtensions for Instrumentation (PXI) specification. It also defines the intended audience and lists relevant terminology and documents.

1.1 Objectives

PXI was created in response to the needs of a variety of instrumentation and automation users who require ever increasing performance, functionality, and reliability from compact rugged systems that are easy to integrate and use. Existing industry standards are leveraged by PXI to benefit from high component availability at lower costs. Most importantly, by maintaining software compatibility with industry-standard personal computers, PXI allows industrial customers to use the same software tools and environments with which they are familiar.

PXI leverages the electrical features defined by the widely adopted Peripheral Component Interconnect (PCI) specification. It also leverages the CompactPCI form factor, which combines the PCI electrical specification with rugged Eurocard mechanical packaging and high-performance connectors. This combination allows CompactPCI and PXI systems to have up to seven peripheral slots versus four in a desktop PCI system. Systems with more expansion slots can be built by using multiple bus segments with industry-standard PCI-PCI bridges. For example, a 13-slot PXI system can be built using a single PCI-PCI bridge. The PXI Hardware Specification adds electrical features that meet the high-performance requirements of instrumentation applications by providing triggering, local buses, and system clock capabilities. PXI also offers two-way interoperability with CompactPCI products.

By implementing desktop PCI in a rugged form factor, PXI systems can leverage the large base of existing industry-standard software. Desktop PC users have access to different levels of software, from operating systems to low-level device drivers to high-level instrument drivers to complete graphical APIs. All of these software levels can be used in PXI systems. The PXI Systems Alliance maintains a separate Software Specification for PXI modules, chassis, and systems. By having a separate Software Specification, the PXI Systems Alliance can more quickly adopt the latest operating systems and software standards. PXI modules, chassis, and systems developed to comply with this PXI Hardware Specification must also comply with the PXI Software Specification.

Figure 1-1 summarizes the scope of the PXI specification standard by depicting its mechanical, electrical, and software architectures. It also shows how the separate Hardware and Software specifications are partitioned.

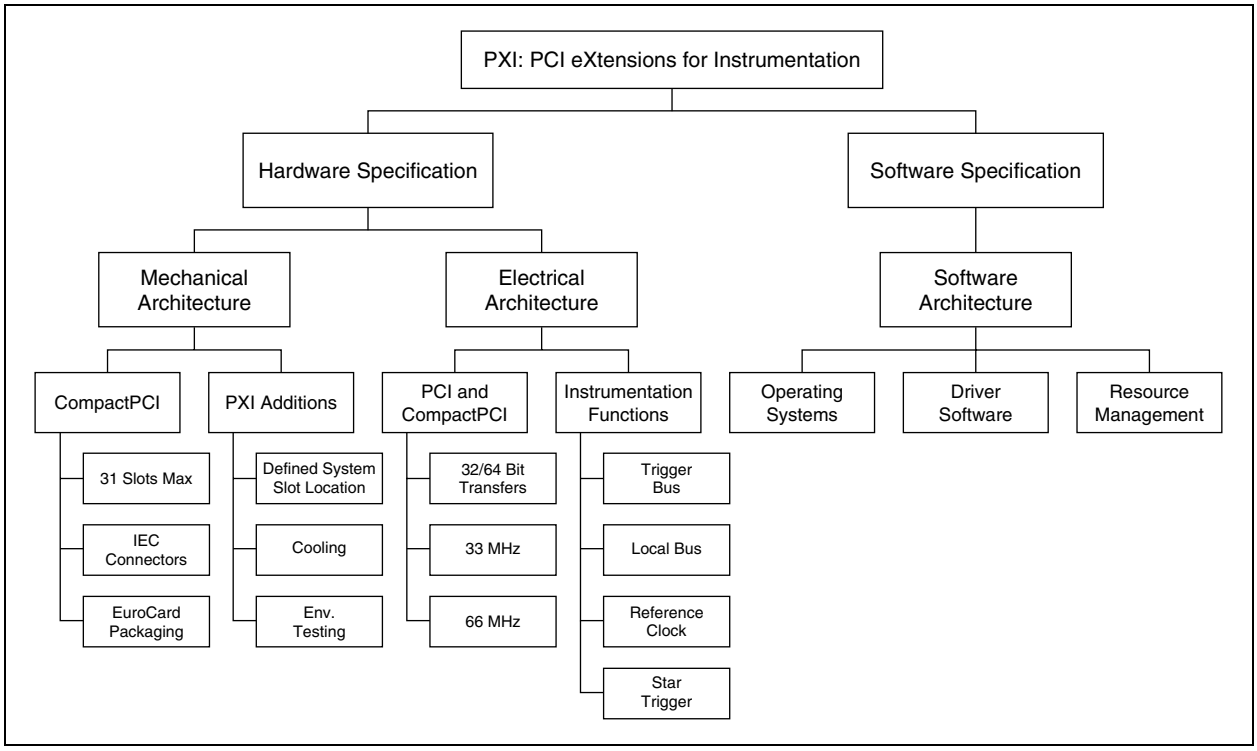

Figure 1-1. The PXI Architecture

1.2 Intended Audience and Scope

This specification is organized with a top-down approach whereby general descriptions precede the more detailed specifications found deeper in the subsections. This structure is intended to serve the needs of a variety of audiences from product developers to system integrators to end-users. Product developers may want to become familiar with all portions of this specification while end users may be interested in only the feature set description and perhaps the summaries of how these features are implemented. The goal of this specification is to serve as the central source of information relevant to all users and providers of PXI compatible systems.

The first section of this specification describes the features that PXI systems can offer and how these features can be applied to instrumentation. The subsequent sections cover the mechanical, electrical, and software requirements specific to implementing PXI features.

1.3 Background and Terminology

This section defines the acronyms and key words that are referred to throughout this specification.
This specification uses the following acronyms:

- **API**—Application Programming Interface
- **CompactPCI**—PICMG 2.0 Specification
- **Eurocard**—European Packaging Specifications (IEC 60297, IEEE 1101.1, IEEE 1101.10, IEEE 1101.11)
- **GPIB**—General Purpose Interface Bus, IEEE 488

- **ISA**—Industry Standard Architecture; desktop PC adapter board specification
- **PCI**—Peripheral Component Interconnect; electrical specification defined by PCISIG
- **PCISIG**—PCI Special Interest Group
- **PICMG**—PCI Industrial Computer Manufacturers Group
- **PXI**—PCI eXtensions for Instrumentation
- **VISA**—Virtual Instrument Software Architecture
- **VITA**—VMEbus International Trade Association
- **VME**—Versa Module Europe; VMEbus specification governed by the VSO
- **VPP**—VXI*plug&play* Specification
- **VSO**—VITA Standards Organization
- **VXI**—VME Extensions for Instrumentation

This specification uses several key words, which are defined as follows:

RULE: Rules SHALL be followed to ensure compatibility. A rule is characterized by the use of the words SHALL and SHALL NOT.

RECOMMENDATION: Recommendations consist of advice to implementers that will affect the usability of the final module. A recommendation is characterized by the use of the words SHOULD and SHOULD NOT.

PERMISSION: Permissions clarify the areas of the specification that are not specifically prohibited. Permissions reassure the reader that a certain approach is acceptable and will cause no problems. A permission is characterized by the use of the word MAY.

OBSERVATION: Observations spell out implications of rules and bring attention to things that might otherwise be overlooked. They also give the rationale behind certain rules, so that the reader understands why the rule must be followed.

MAY: A key word indicating flexibility of choice with no implied preference. This word is usually associated with a permission.

SHALL: A key word indicating a mandatory requirement. Designers SHALL implement such mandatory requirements to ensure interchangeability and to claim conformance with the specification. This word is usually associated with a rule.

SHOULD: A key word indicating flexibility of choice with a strongly preferred implementation. This word is usually associated with a recommendation.

1.4 Applicable Documents

This specification defines extensions to the base PCI and CompactPCI specifications referenced in this section. It is assumed that the reader has a thorough understanding of PCI and CompactPCI. The CompactPCI specification refers to several other applicable documents with which the reader may wish to become familiar. This specification refers to the following documents directly:

- *PXI Software Specification (Latest Revision)*
- *PCI Local Bus Specification*, Rev. 2.3
- PICMG 2.0 R3.0 CompactPCI Specification
- VXI*plug&play* Specifications (VPP-3.*x* and VPP-7)

- IEC 61326-1:1997, *Electrical equipment for measurement, control, and laboratory use—EMC requirements—Part I, General requirements*, International Electrotechnical Commission
- IEC 1010-1:1990 + A1:1992, *Safety requirements for electrical equipment for measurement, control, and laboratory use—Part 1, General requirements*, International Electrotechnical Commission
- IEC 60068-1, *Environmental testing*, International Electrotechnical Commission

1.5 Useful Web Sites

Below is a list of web site links that at the time of publication of this specification point to sites with information useful in the understanding and design of PXI products.

`http://www.pxisa.org/`	PXI specifications
`http://www.picmg.org/`	PICMG specifications
`http://www.ieee.org/`	IEEE specifications
`http://www.iec.org/`	IEC specifications
`http://www.pcisig.com/`	PCI specifications
`http://www.vita.com/`	VME specifications
`http://www.vxi.org/`	VXI specifications
`http://www.vxipnp.org/`	VISA specifications

2. PXI Architecture Overview

This section presents an overview of a PXI system features and capabilities by summarizing the mechanical, electrical and software architectures defined by this specification.

2.1 Mechanical Architecture Overview

PXI supports the two module form factors that are depicted in Figure 2-1. The 3U module form factor defines modules that are 100 by 160 mm (3.94 by 6.3 in.) and have two interface connectors. J1 carries the signals required for the 32-bit PCI local bus and J2 carries the signals for 64-bit PCI transfers and the signals for implementing PXI electrical features. The 6U peripheral module form factor defines modules that are 233.35 by 160 mm (9.19 by 6.3 in.) and in the future may carry one additional connector for expansion of the PXI Hardware Specification. 6U system modules and system slots may use P3/J3, P4/J4, P5/J5 for rear I/O purposes.

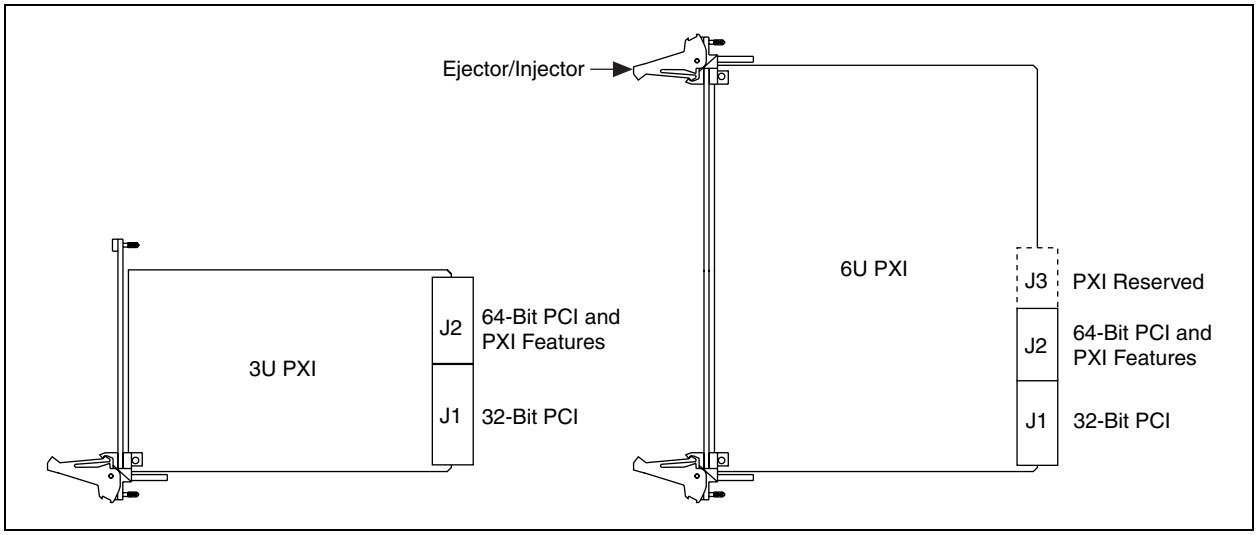

Figure 2-1. PXI Peripheral Module Form Factors and Connectors

Figure 2-2 presents an example of a typical PXI system to help illustrate the following keywords (in *italics*). A PXI system is composed of a *chassis* that supports the PXI *backplane* and provides the means for supporting the *system controller module* and the *peripheral modules*. The chassis must have one *system slot* and may have one or more *peripheral slots*. Any number of *controller expansion slots* may be available to the left of the system slot. The optional *star trigger controller*, when used, must reside next to the system controller module. If a star trigger controller is not used in a system, a peripheral module can be installed in the slot next to the system controller module. The backplane carries the *interface connectors* (P1, P2, ...) and provides the interconnection between the controller and peripheral modules. A maximum of seven peripheral modules can be used in a single 33 MHz PXI *bus segment, and a maximum of 4 peripheral modules can be used in a single 66 MHz PXI bus segment*. PCI-PCI bridges can be used to add bus segments for additional peripheral slots.

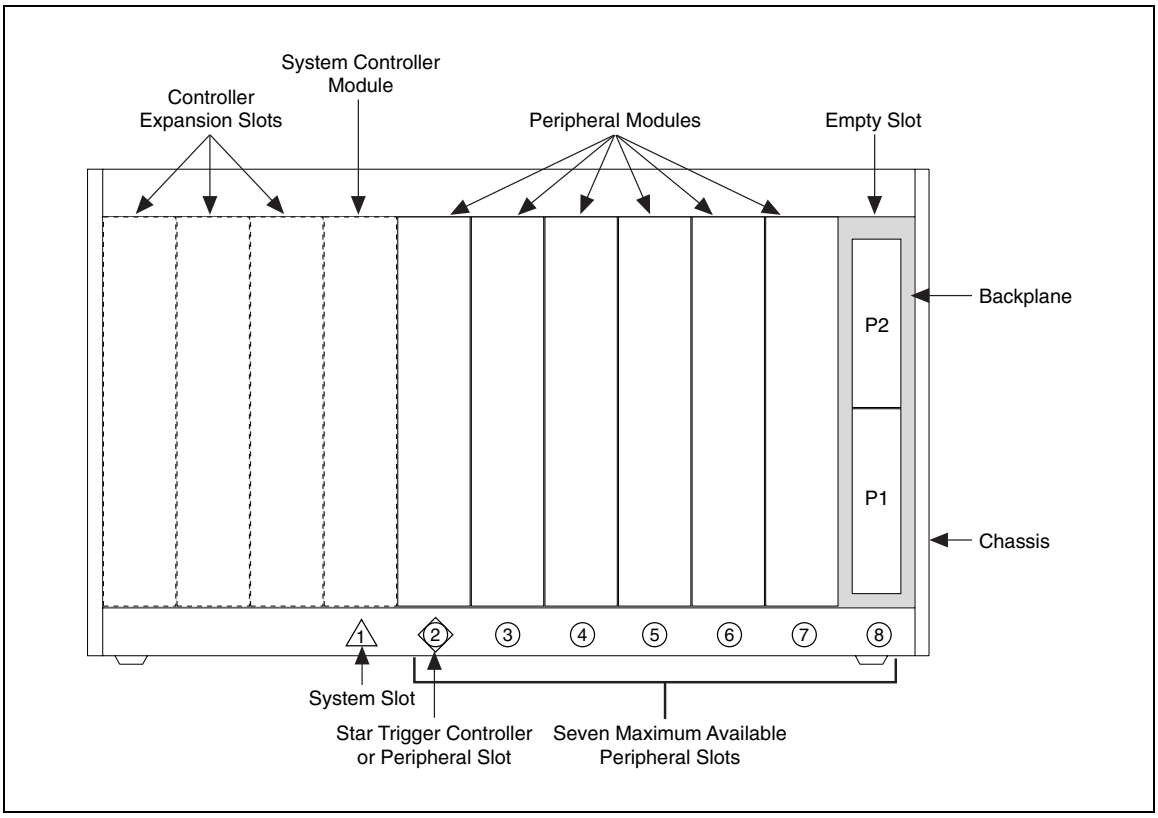

Figure 2-2. Example of a 33 MHz 3U PXI System (Single Bus Segment)

2.1.1 Chassis Supporting Stacking 3U Modules in a 6U Slot

For efficient use of 3U modules in a 6U chassis, 6U chassis can support stacking two 3U modules in a single 6U slot. This allows one 3U module to be plugged into the P1/P2 position of a 6U slot and another 3U module to be plugged into the P4//P5 position of the same 6U slot simultaneously. A 6U PXI chassis may have any number of 6U slots that support this feature.

Electrically this configuration is accomplished by populating connectors in the P4 and P5 positions of the 6U backplane and routing them as you would P1/P2. PCI bridging is required on the 6U backplane between the PCI bus residing on the P1 and P2 connectors and the PCI bus residing on the P4 and P5 connectors if PCI bus length and loading requirements can not be met. PCI bridging between the PCI bus residing on the P1 and P2 connectors and the PCI bus residing on the P4 and P5 connectors is not allowed on the system controller module.

Mechanically this configuration can be accomplished by making use of center extrusions fixed within the chassis to physically support the insertion, extraction, and mounting of the lower and upper 3U modules residing in a 6U slot. Alternatively, this may accomplished mechanically by a stacking adapter attached to the two 3U modules prior to insertion into the 6U slot. Figure 2-3 shows an example of a 6U chassis that supports stacking 3U modules.

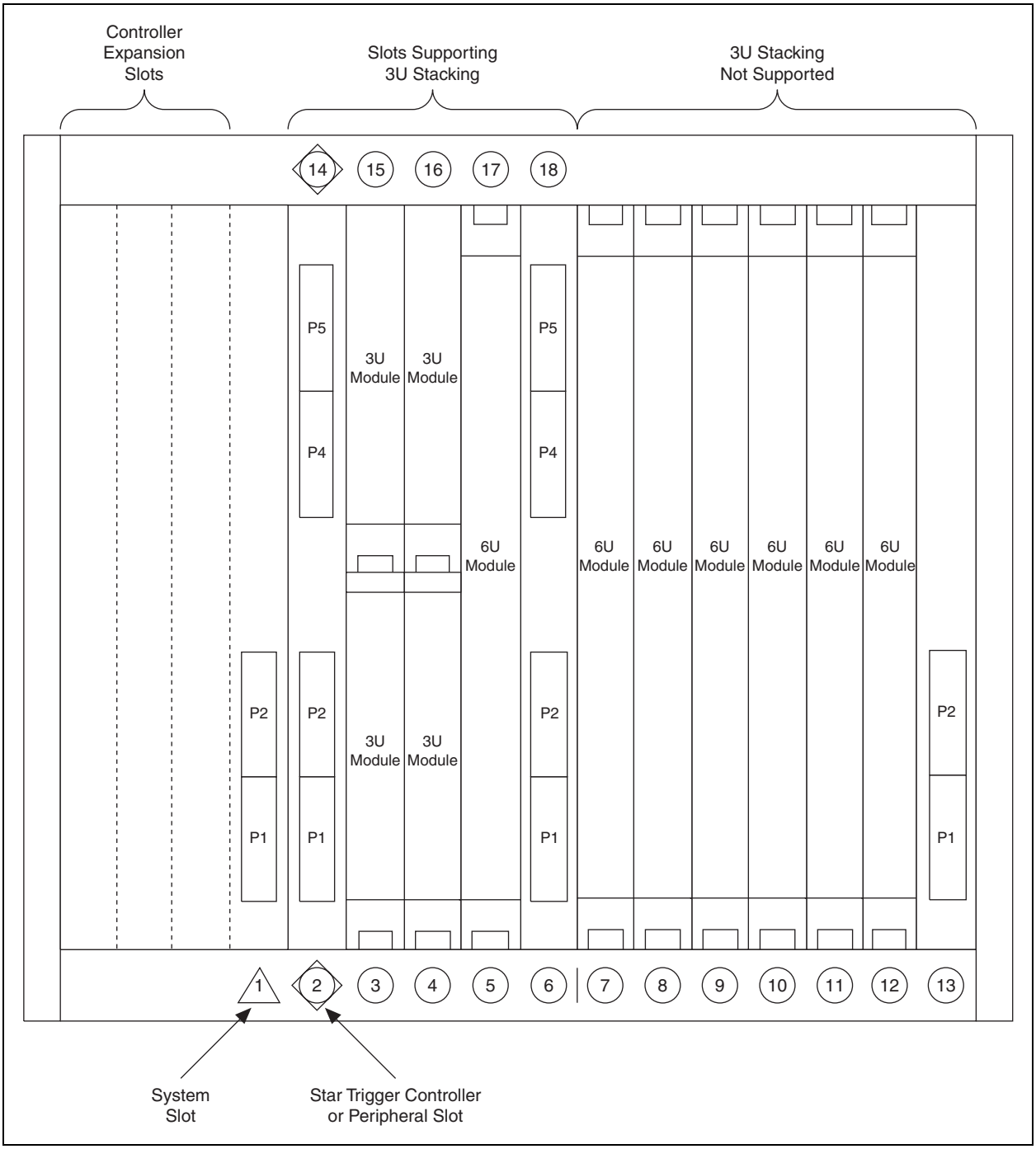

Figure 2-3. Example of a 6U Chassis that Supports Stacking 3U Modules

2.1.2 System Slot Location

PXI defines the system slot location to be on the left end of the PCI bus segment in a basic PXI system. This defined arrangement is a subset of the numerous possible configurations allowed by CompactPCI (a CompactPCI system slot may be located anywhere on a backplane). Defining a single location for the system slot simplifies integration and increases the degree of compatibility between PXI controllers and chassis. Furthermore, the PXI Hardware Specification requires that if necessary the system controller module

should expand to the left into what are defined as controller expansion slots. Expanding to the left prevents system controllers from using up valuable peripheral slots.

PXI also defines the location of a star trigger controller slot that can accept a peripheral module or a special star trigger module that can provide individual triggers to all other peripheral modules. The star trigger signals are routed from the star trigger slot to each peripheral slot on all PXI backplanes.

2.1.3 Additional Mechanical Features

All mechanical specifications defined in PICMG 2.0 R3.0 (CompactPCI Specification) apply directly to PXI systems; however, PXI includes additional requirements that simplify system integration. Forced cooling in a PXI chassis is required and the airflow direction is defined. Environmental testing for operating and storage temperature ratings of all PXI products is required and must be clearly documented by suppliers.

2.1.4 Interoperability with CompactPCI

Interoperability among PXI compatible products and standard CompactPCI products is a very important feature provided by this specification. Many PXI-compatible systems will require components that do not implement PXI-specific features. For example, a user may want to use a standard CompactPCI network interface module in a PXI chassis. Likewise, some users may choose to use a PXI compatible module in a standard CompactPCI chassis. In these cases, the user will not be able to use PXI-specific functions but will still be able to use the basic functions of the module. Note that interoperability between PXI-compatible products that use the J2 connector for PXI-defined signals and other application-specific implementations of CompactPCI chassis (which may define other signal definitions for sub-buses on the P2 backplane connector) is not guaranteed. Of course, both CompactPCI and PXI leverage the PCI local bus, thereby ensuring software and electrical compatibility as depicted in Figure 2-4.

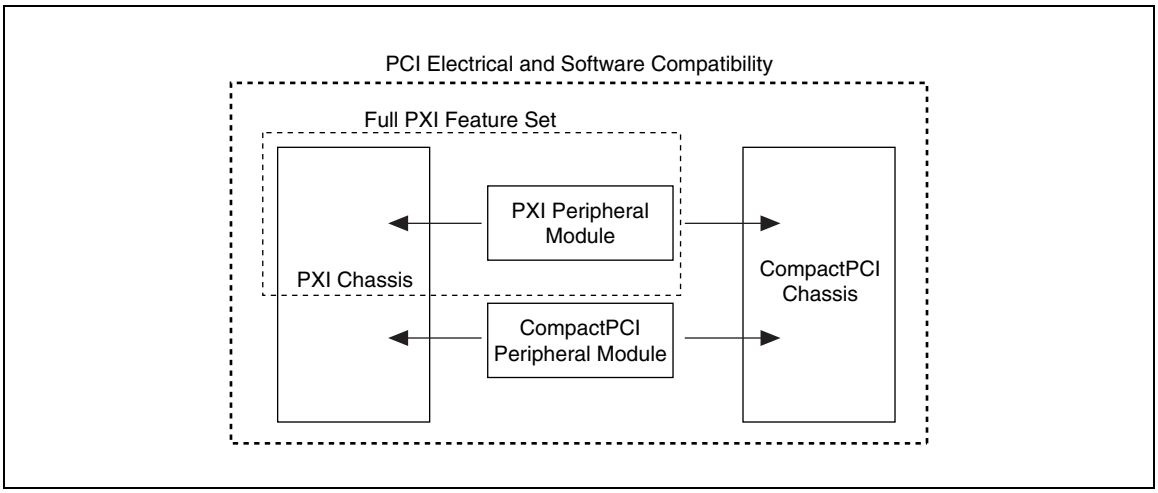

Figure 2-4. PXI and CompactPCI Interoperability

2.2 Electrical Architecture Overview

Many instrumentation applications require system timing capabilities that cannot be directly implemented across standard desktop computer backplanes such as ISA, PCI, or PCMCIA. PXI uses the standard PCI bus and adds specific signals for instrumentation including bused trigger lines, slot-specific triggers, a dedicated system clock, and slot-to-slot local buses to address the need for advanced timing, synchronization, and side-band communication.

2.2.1 Peripheral Component Interconnect (PCI) Features

PXI offers the same performance features defined by the desktop PCI specification, with one notable exception. A PXI system can have up to eight slots per 33 MHz segment (one system slot and seven peripheral slots), whereas a desktop PCI system can have only five per 33 MHz segment (one motherboard or system slot and four peripheral slots). Similarly, a PXI system can have up to five slots per 66 MHz segment (one system slot and four peripheral slots), whereas a desktop PCI system can have only three per 66 MHz segment (one motherboard or system slot and two peripheral slots). The capability to have three additional 33 MHz peripheral slots and two additional 66 MHz peripheral slots is defined in the CompactPCI specification upon which PXI draws. Otherwise, all the features of PCI transfer into PXI:

- 33/66 MHz performance
- 32-bit and 64-bit data transfers
- 132 Mbytes/s (32-bit, 33MHz) to 528 Mbytes/s (64-bit, 66 MHz) peak data rates
- System expansion via PCI-PCI bridges
- 3.3V migration
- Plug and Play capability

Similar to the PCI specification, it is recommended that PXI modules do not have their internal registers mapped to PCI I/O Space. I/O Space is limited, fragmented, and increasingly more difficult to guarantee allocation.

2.2.2 Local Bus

The PXI local bus is a daisy-chained bus that connects each peripheral slot with its adjacent peripheral slots to the left and right. Thus, the right local bus of a given peripheral slot connects to the left local bus of the adjacent slot, and so on. Each local bus is 13 lines wide and can be used to pass analog signals between modules or to provide a high-speed side-band digital communication path that does not affect the PXI bandwidth.

Local bus signals can range from high-speed TTL signals to analog signals as high as 42 V. Keying of adjacent modules is implemented by initialization software that prohibits the use of incompatible modules. This software uses the configuration information specific to each peripheral module to evaluate compatibility before enabling local bus circuitry. This method provides a flexible means for defining local bus functionality that is not limited by hardware keying.

The local bus lines for the leftmost peripheral slot of a PXI backplane are used for the star trigger. Figure 2-5 schematically shows a complete PXI system demonstrating the local buses.

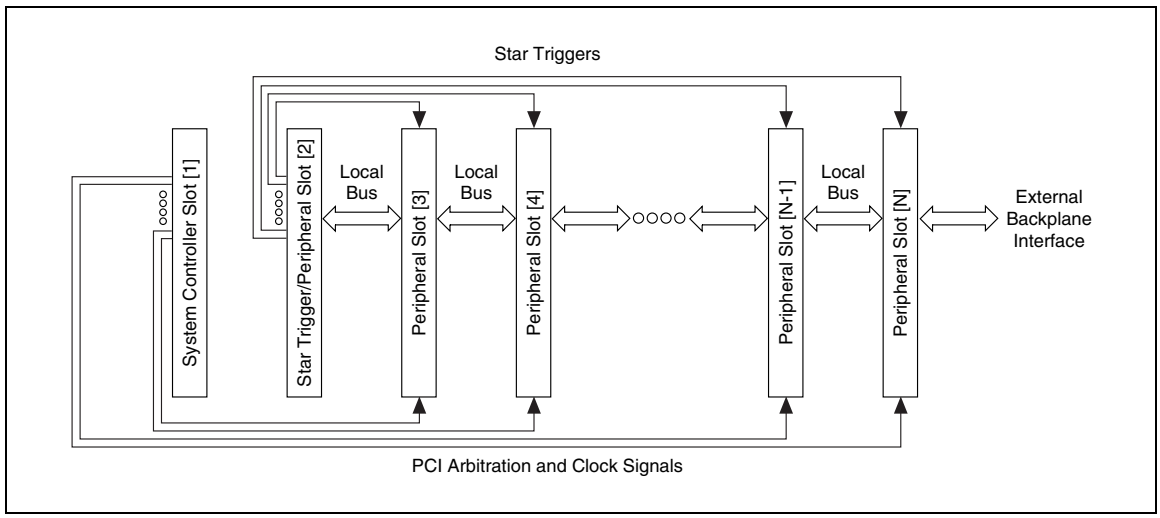

Figure 2-5. PXI Local Bus Routing

2.2.3 System Reference Clock

The PXI 10 MHz system clock (PXI_CLK10) is distributed to all peripheral modules in a system. This common reference clock can be used for synchronization of multiple modules in a measurement or control system. The PXI backplane specification defines implementation guidelines for PXI_CLK10. As a result, the low skew qualities afforded by this reference clock make it ideal for precise multimodule synchronization by using trigger bus protocols to qualify individual clock edges.

2.2.4 Trigger Bus

The eight PXI bused trigger lines are highly flexible and can be used in a variety of ways. For example, triggers can be used to synchronize the operation of several different PXI peripheral modules. In other applications, one module can control carefully timed sequences of operations performed on other modules in the system. Triggers may be passed from one module to another, allowing precisely timed responses to asynchronous external events that are being monitored or controlled. The number of triggers that a particular application requires varies with the complexity and number of events involved.

2.2.5 Star Trigger

The PXI star trigger bus offers ultra-high performance synchronization features to users of PXI systems. The star trigger bus implements a dedicated trigger line between the first peripheral slot (adjacent to the system slot) and the other peripheral slots. A star trigger controller can be installed in this slot and can be used to provide very precise trigger signals to other peripheral modules. Systems that do not require this advanced trigger can install any standard peripheral module in this slot. Through the required use of line-length equalization techniques for routing the star triggers, PXI systems can meet demanding triggering requirements for which bused triggers are not appropriate. Note that the star trigger can be used to communicate information back to the star trigger controller, as in the case of reporting a slot's status, as well as responding to information provided by the star trigger controller.

This trigger architecture for PXI gives two unique advantages in augmenting the bused trigger lines. The first advantage is a guarantee of a unique trigger line for each module in the system. For large systems, this eliminates the need to combine multiple module functions on a single trigger line or to artificially limit the number of trigger times available. The second advantage is the low-skew connection from a single trigger

point. The PXI backplane defines specific layout requirements such that the star trigger lines provide matched propagation time from the star trigger slot to each module for very precise trigger relationships between each module.

2.2.6 System Expansion with PCI-PCI Bridge Technology

A PXI system can be built with more than one bus segment by using standard PCI-PCI bridge technology. The bridge device takes up one PCI load on each of the bus segments that it links together. Thus, a 33 MHz system with two bus segments offers 13 expansion slots for PXI peripheral modules.

(2 bus segments) × (8 slots per segment) – (1 system controller slot)
– (2 slots for PCI-PCI Bridge) = 13 available expansion slots

Similarly, a three-bus segment 33 MHz system would offer 19 expansion slots for PXI peripheral modules.

The trigger architecture defined by PXI has implications for systems with multiple bus segments. The PXI trigger bus provides connectivity within a single bus segment and does not allow physical connection to an adjacent bus segment. This maintains the high performance characteristics of the trigger bus and allows multisegment systems to partition instruments into logical groups. Multiple segments may be logically linked by providing buffers between physical segments. The star trigger provides the means to independently access all 13 peripheral slots in a two-segment system for applications in which a high number of instruments require synchronization and controlled timing. In PXI systems where there are more than two segments, it is recommended that the star triggers are only routed to the slots in the first two segments, but other routings are allowed. Figure 2-6 shows the PXI trigger architecture for a PXI system with two bus segments.

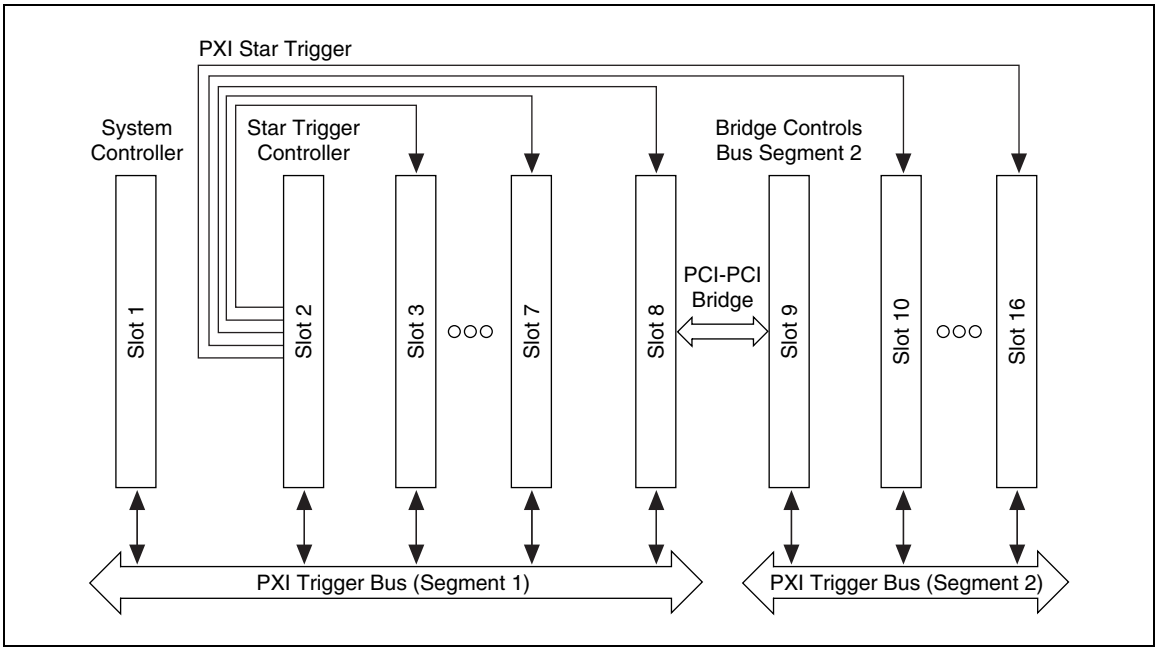

Figure 2-6. PXI Trigger Architecture for Two Bus Segments

2.2.7 32-bit PCI and Rear I/O

Many PXI modules only require 32-bit PCI support which could be used in lower cost chassis that do not support 64-bit PCI. Additionally since the upper 32-bit PCI signals will not be used in these chassis, suppliers of PXI chassis may decide to use these signals for rear I/O purposes on the system slot. Section 6 of this specification defines chassis that do not support 64-bit PCI. It also defines system controller modules which support supplier specific rear I/O.

2.3 Software Architecture Overview

Revision 2.0 and earlier of the PXI Specification included software requirements for PXI modules, chassis and systems. From PXI Hardware Specification revision 2.1 and higher, the PXI Systems Alliance maintains a separate software specification for PXI modules, chassis and systems. PXI modules, chassis, and systems developed to comply with this PXI Hardware Specification must also comply with the PXI Software Specification. The Software Architecture Overview is now covered in the PXI Software Specification.

3. Mechanical Requirements

This section discusses the additional mechanical requirements for PXI systems. It discusses the location of the system slot, the interoperability of the controller with the chassis, the PXI logo, environmental testing, cooling, grounding, and guidelines for minimizing electromagnetic interference (EMI).

3.1 CompactPCI Mechanical Requirements

Both 3U (100 by 160 mm, or 3.94 by 6.3 in.) and 6U (233.35 by 160 mm, or 9.19 by 6.3 in.) form factor modules can implement PXI features as defined in Section 4, *Electrical Requirements*.

RULE: All mechanical requirements defined in the CompactPCI specification (PICMG 2.0 R3.0) SHALL apply to 3U and 6U PXI compatible modules.

The following sections define additional mechanical requirements and recommendations that are included to ease system integration.

3.2 Maximum Number of Slots

Since the CompactPCI specification accommodates 31 slots based on the definition of the Geographical Addressing pins, it is necessary to limit a PXI chassis to 31 slots.

RULE: A PXI chassis SHALL NOT have more than 31 slots.

3.3 System Slot Location and Rules

All CompactPCI and PXI compatible systems require a backplane/chassis and a system controller module in the system slot. This requirement allows users to mix and match different controllers with different chassis. However, because the CompactPCI specification allows a system slot to be located anywhere relative to peripheral slots, the possibility for confusion and incompatibility exists. To address this problem the following rules must be followed for PXI-compatible systems:

RULE: The system slot SHALL be defined as the leftmost PXI slot in a basic single bus segment PXI chassis/backplane. For documentation purposes this slot is counted as one *controller* slot.

RECOMMENDATION: If the system controller module requires more than one slot width, it SHOULD extend to the LEFT of the system slot in full slot increments (one slot equals 20.32 mm, or 0.8 in.) into additional controller expansion slots.

OBSERVATION: In a basic PXI system these additional controller slots are for physical expansion of the system controller module only and cannot support peripheral modules. These slots DO NOT have connectors that interface to the PCI bus routed on the backplane.

OBSERVATION: Extending the system slot module to the LEFT allows all PXI peripheral slots to be utilized.

RECOMMENDATION: The system controller module SHOULD NOT extend to the RIGHT of the system slot into peripheral slots.

OBSERVATION: If a system controller module expands to the right, the number of usable PXI peripheral slots may be compromised and access to the star trigger slot may be eliminated.

RULE: Every PXI system controller module SHALL clearly document how many controller expansion slots (to the left of the system slot) and peripheral slots it occupies.

RULE: Every PXI chassis SHALL clearly document how many peripheral and controller expansion slots are available.

OBSERVATION: The two preceding rules help ensure that end users can easily determine whether a particular controller-chassis pair is compatible and how many peripheral slots are available.

Figure 3-1 depicts slot designations in a PXI system.

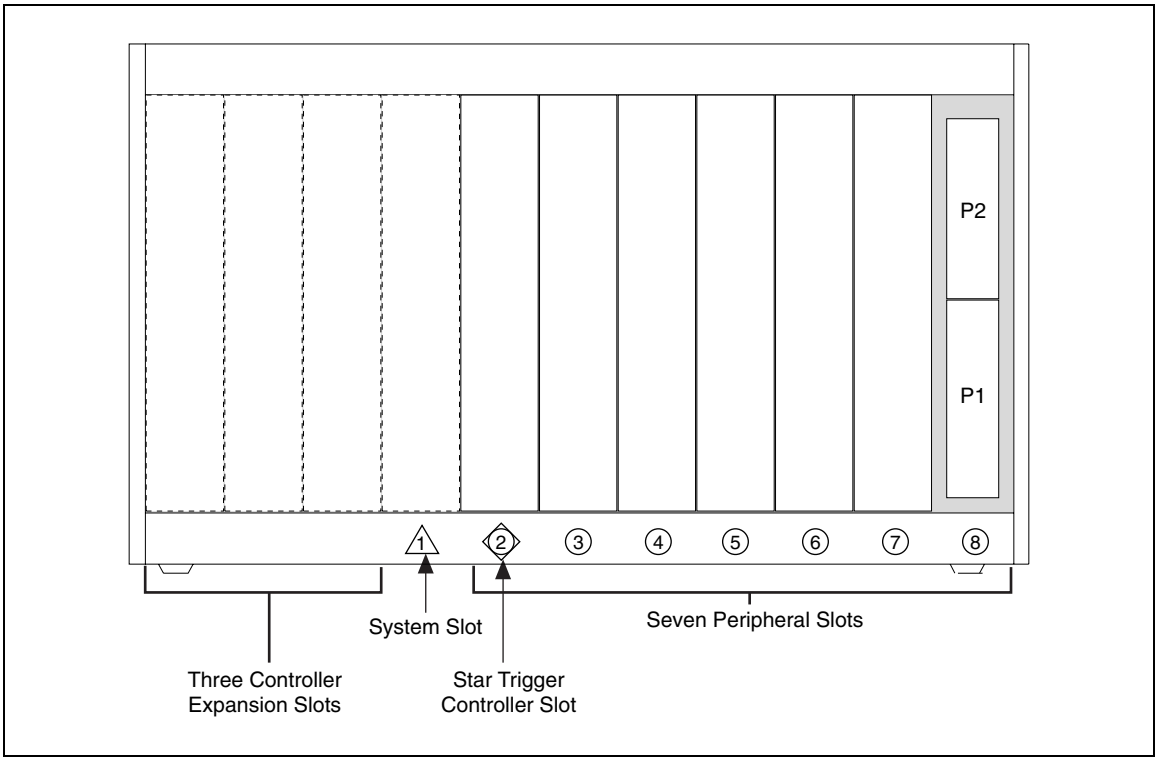

Figure 3-1. Example of PXI Slot Designations for a Chassis

3.4 Logos and Compatibility Glyphs

RULE: A PXI chassis SHALL clearly mark each physical slot with a unique number. The number SHALL be located within the compatibility glyph.

OBSERVATION: The preceding rule applies to a chassis with multiple bus segments as well as to a single-segment chassis.

PERMISSION: Vendors who are members of the PXI Systems Alliance MAY use the PXI logo as defined below on either the front panel or the injector/ejector handle of products claiming full compliance with the PXI Hardware Specification.

RULE: If the PXI logo is used, the vendor SHALL license the trademarked logo.

RULE: If the PXI logo is used, it SHALL NOT be altered in any way other than scale. The logo SHALL NOT incorporate any additions.

Figure 3-2 shows the PXI logo. Logo artwork as well as the license can be obtained from the PXI Systems Alliance once becoming a member.

Figure 3-2. PXI Logo

PERMISSION: The PXI logo MAY be used as a substitute for the CompactPCI logo defined in PICMG 2.0 R3.0. Additionally, a product MAY display both the CompactPCI logo and the PXI logo.

RULE: Modules and backplanes SHALL use the compatibility glyphs as defined in the PICMG 2.0 R3.0 (CompactPCI specification).

RULE: Modules and backplanes SHALL use the glyph shown in Figure 3-3 (square at 45°) for the star trigger slot/module. This slot is always located next to the system slot. Because this slot can also support standard peripheral modules, the peripheral module glyph (circle) SHALL also be used for this slot.

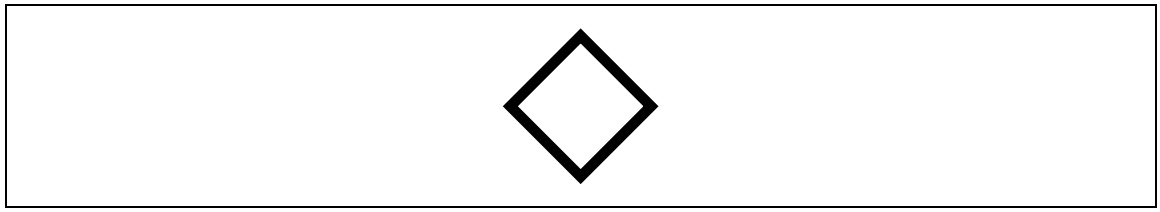

Figure 3-3. Star Trigger Slot Glyph

RULE: Chassis and backplanes SHALL use the glyph shown in Figure 3-4 (vertical line) between slot numbers to indicate boundaries between PCI segments.

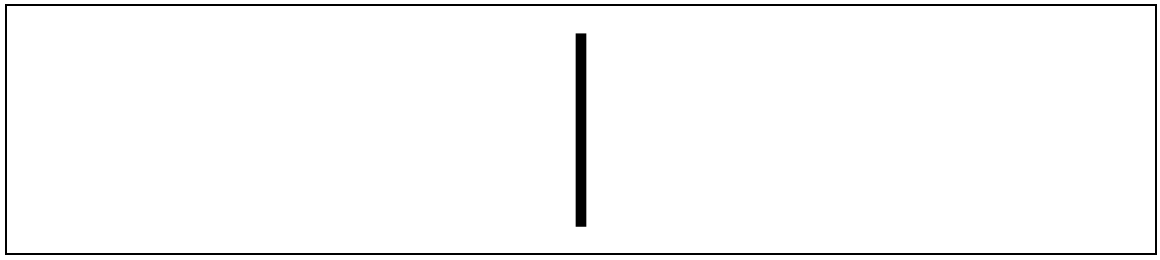

Figure 3-4. PCI Segment Divider Glyph

3.5 Slot Numbering for 6U Chassis that Support 3U Stacking

The CompactPCI specification does not define chassis that support stacking 3U modules in a 6U slot. To make physical slot numbering of these systems explicit, the following rule applies:

RULE: 6U PXI Chassis that support stacking 3U modules in a 6U slot SHALL have their slots numbered, starting with the furthest slot to the left, with the number 1 below the slot. Continuing from left to right, the slots numbers SHALL be incremented by one until all slots have been numbered below the slot. Slots that support stacking 3U modules (P4 and P5 populated) SHALL have a number above the slot starting with one number higher than the highest number used below all the slots. Continuing from left to right on slots that

support stacking 3U modules, the slot numbers SHALL be incremented by one until all slots that support stacking 3U modules have been numbered above the slot.

OBSERVATION: 6U PXI Chassis that support stacking 3U modules will not have slot numbers above slots that do not support stacking 3U modules.

Figure 3-5 depicts the slot numbering for a 6U chassis that supports stacking 3U modules.

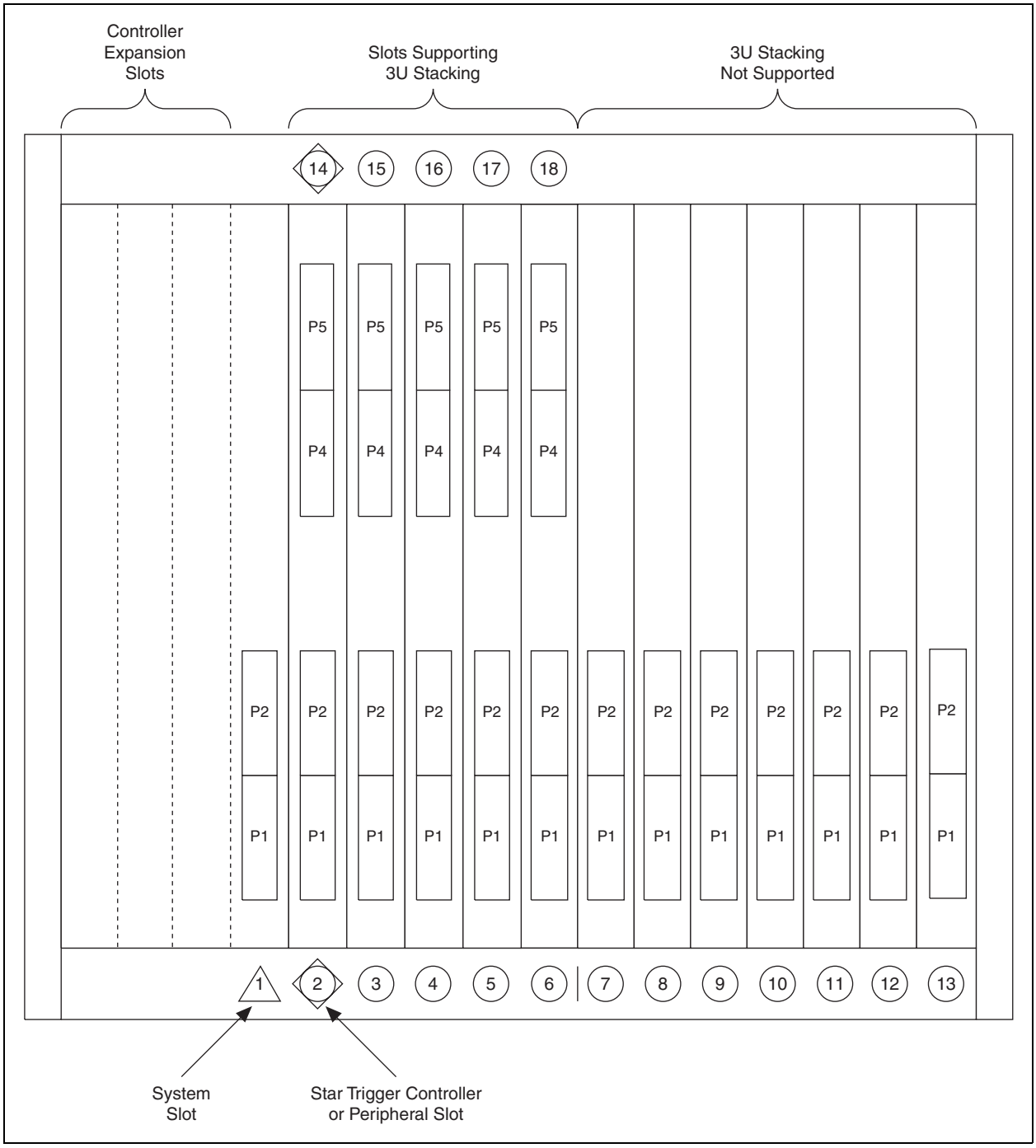

Figure 3-5. Example of Slot Numbering for a 6U Chassis that Supports 3U Stacking

3.6 Environmental Testing

RULE: PXI chassis, system controller modules, and peripheral modules SHALL be tested for storage and operating temperature ranges.

RECOMMENDATION: PXI chassis, system controller modules, and peripheral modules SHOULD be tested for humidity, vibration, and shock.

RECOMMENDATION: All environmental testing SHOULD be carried out according to the procedures described in IEC 60068.

RULE: Test results and reports generated for environmental testing SHALL be made available to end users of PXI systems. All manufacturers of PXI chassis, system controller modules, and peripheral modules SHALL supply operating and storage temperature ratings for their products.

RULE: If a manufacturer chooses to use environmental testing procedures other than those described in IEC 60068, then these procedures, in addition to the test results and reports, SHALL be documented and made available to the customer.

OBSERVATION: It is the system integrator's responsibility to select modules and chassis appropriate for the application's environmental requirements.

3.7 Cooling Specifications

3.7.1 Plug-in Module Requirements

RULE: Plug-in modules SHALL be designed to allow a suitable airflow path from bottom to top as shown in Figure 3-6.

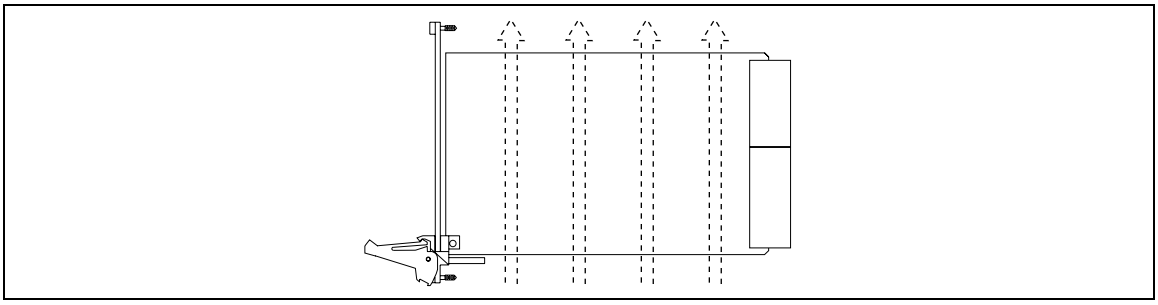

Figure 3-6. Cooling Airflow Direction in a PXI System

RULE: Plug-in module manufacturers SHALL document and make available to the customer the nominal wattage generated by the module under normal operating conditions.

RECOMMENDATION: Single width 3U plug-in modules SHOULD NOT dissipate within the chassis more than 25 watts.

RECOMMENDATION: Single width 6U plug-in modules SHOULD NOT dissipate within the chassis more than 50 watts.

3.7.2 Chassis Requirements

RULE: Chassis SHALL provide active cooling that flows from the bottom to the top of a plugged-in module as shown in Figure 3-6.

RULE: Chassis manufacturers SHALL document and make available to the customer the maximum total wattage that a given chassis can dissipate and the maximum wattage dissipated for the worst-case slot. Furthermore, the manufacturer SHALL document and make available to the customer the specific test procedure used to determine these wattage values.

RULE: PXI chassis SHALL have filler panels installed in slots that do not have modules populated.

OBSERVATION: If filler panels are not installed in slots that do not have modules populated, then proper module cooling can not be guaranteed.

3.8 Chassis and Module Grounding Requirements and EMI Guidelines

RULE: Chassis SHALL provide a direct (low-impedance) means for connecting the chassis ground to earth ground.

OBSERVATION: A grounding stud may be used to provide direct access to chassis ground.

RECOMMENDATION: As defined in PICMG 2.0 R3.0, PXI modules SHOULD use metalized shell connectors for EMI/RFI protection. The shell SHOULD be electrically connected to the front panel through a low impedance path in accordance with IEEE 1101.10.

RECOMMENDATION: PXI modules SHOULD be grounded according to the recommendations contained in Section 4.4.

3.9 Regulatory Requirements

The following standards assure uniform performance and international portability of PXI systems and modules. Allowances are made for devices not intended for international sale. All regulatory compliance information must be clearly documented for the user. Subsequently issued standards or amendments to these standards shall apply.

3.9.1 Requirements for EMC

RULE: Testing SHALL be performed, either by the manufacturer or a competent laboratory, marked accordingly, and documented showing compliance to the following EMC standard(s).

IEC 61326-1:1998, *Electrical equipment for measurement, control, and laboratory use—EMC requirements—Part I, General requirements*[1]:

- Localized EMC standards may be substituted if sale and use are restricted accordingly.[2]
- Use current edition of EN 55011, Group 1, Class A or Class B Limits, at 10 m.
- Continuous unmonitored operation is assumed unless otherwise specified by manufacturer.

[1] At the time of this writing, IEC 61326-1 was not yet normalized for CE Marking, but its first edition has been published by the IEC as a bonafide standard. The ISM emission and generic immunity standards may be substituted during any legally allowed transition period if documented accordingly.

[2] The use of localized EMC or safety standards must be clearly documented for the benefit of the user. The standards used may include standards in force during legally allowed transitional periods of new standards or amendments. Currently, manufacturer declarations must list all standards used for declaring compliance and conveniently meet this requirement when the declarations are included with the user documentation.

3.9.2 Requirements for Electrical Safety

RULE: Testing SHALL be performed, either by a competent organization or qualified manufacturer, marked accordingly, and documented showing compliance to the following electrical safety standard(s). Strictly extra low voltage (SELV) devices do not need formal agency testing, though the basic requirements still apply, such as material flammability specified, DC power outputs fused or limited, and so on.

IEC 1010-1:1990 + A1:1992, *Safety requirements for electrical equipment for measurement, control, and laboratory use—Part 1, General requirements*:

- IEC 950 and amendments are acceptable for applications restricted to the office use only.
- Localized safety standards may be substituted if sale and use are restricted accordingly.[2]

3.9.3 Additional Requirements for Chassis

RULE: Chassis manufacturers, or a designated party, SHALL demonstrate EMC compliance with a commonly available controller. At minimum the controller SHALL apply a 33 MHz clock to the backplane, or higher as the technology commonly supports, unless the marketing and use of the chassis is restricted to specific kinds of system controllers or platforms. A reasonably common processor speed is sufficient for this test. The complete controller system, including hard drive, floppy drive, serial, parallel, keyboard, mouse, and video ports (as offered with the controller) will be exercised with typical peripherals. Filling remaining slots, if any, is not required. Special shielding or suppression options, if used to achieve compliance, SHALL be documented and available to the user.

RULE: The chassis SHALL be qualified for electrical safety as listed previously. Manufacturer claims of safety compliance are not sufficient without independent verification and regular inspection by a competent agency.

4. Electrical Requirements

This chapter discusses the detailed electrical requirements for developing PXI-compatible peripheral modules, controllers, and backplanes. It discusses all signals required for PXI systems and their related implementation requirements. It also discusses appropriate connector pinouts, power supply requirements, and 6U form factor implementation issues.

4.1 PXI Signal Groups

This section details all the signals required for PXI systems, including those mapped directly from CompactPCI on P1/J1, the 64-bit signals duplicated on P2/J2, and the PXI-specific signals located on P2/J2. The PXI-specific signals include those required for the trigger bus, the reference clock, the local buses, and the star trigger.

4.1.1 P1/J1: Signals

RULE: All signals on the J1 connector of a PXI module and the mating P1 connector of a PXI backplane SHALL meet all the requirements of the PICMG 2.0 R3.0 specification (CompactPCI) for both peripheral modules and system modules.

In order for a system controller module to function correctly in a PXI or CompactPCI system, the BIOS of the controller must have its interrupt routing table configured to allow for the AD[25:31] to IDSEL mapping and associated PCI interrupt routing that is defined in the PICMG 2.0 R3.0 specification (CompactPCI). Connecting the IDSEL lines of backplane PCI devices or PCI-PCI bridges on the first PCI segment to address lines other than AD[25:31] or not connecting these devices to the correct ordering of PCI interrupt lines could cause the PXI or CompactPCI system to function incorrectly. Also, since the PCI-PCI bridge specification was written assuming a bridge would be placed on a PCI plug in card, care must be taken to route the interrupts on the secondary side of the bridge depending on which AD[25:31] is used for the bridge's IDSEL.

RULE: Backplane PCI devices, PCI-PCI bridges, and peripheral slots on the first PCI segment SHALL have their IDSEL lines connected to one of AD[25:31].

RULE: Backplane PCI devices, PCI-PCI bridges, and peripheral slots on the first PCI segment SHALL have their INTA#, INTB#, INTC#, and INTD# pins routed to the system slot's INTA#, INTB#, INTC#, INTD# pins depending on which AD[25:31] line their IDSEL line is connected to in accordance with the PICMG 2.0 R3.0 specification (CompactPCI).

4.1.2 P2/J2: Signals

The PICMG 2.0 R3.0 (CompactPCI) specification defines an open pinout for P2/J2, which allows for custom back-panel I/O implementations. This pinout allows sub-buses on the P2 section of the backplane.

The PXI back-panel I/O definition of signals on the P2/J2 connector consists of signals mapped from the CompactPCI 64-bit connector pinout and new signals defined by this specification. The only differences between the PXI pinout and the CompactPCI 64-bit connector pinout are on signals that are reserved or not used in the CompactPCI specification (PICMG 2.0 R3.0). Therefore, all modules that meet the requirements of the CompactPCI 64-bit specification will function in a PXI system. Furthermore, all PXI modules will work in a system that meets the requirements of the CompactPCI 64-bit specification, but without the complete set of benefits of PXI.

4.1.2.1 Signals from CompactPCI 64-bit Connector Specification

To allow for applications that require higher bandwidth than 32-bit PCI can provide, PXI has incorporated the pieces of the CompactPCI 64-bit specification that are necessary to support 64-bit operation and has used the remaining resources for instrumentation. This section describes the signals that are mapped from the CompactPCI 64-bit specification. The remaining signals are described in subsequent sections.

System Slot

RULE: The following signals SHALL meet all the requirements of the PICMG 2.0 R3.0 specification for the 64-bit CompactPCI pinout on the system slot: GND, V(I/O), AD[32:63], PAR64, C/BE[4:7]#, DEG#, FAL#, PRST#, SYSEN#, CLK[1:6], GNT[1:6]#, REQ[1:6]#, GA0-GA4, SMB_ALERT#, SMB_SCL, SMB_SDA, and the RSV pins.

RULE: The system slot interface in a PXI system SHALL be as defined in the PICMG 2.0 R3.0 Specification (CompactPCI).

OBSERVATION: The PXI implementation of back-panel I/O uses the pins that are BRSV (bused reserved) in the CompactPCI 64-bit pinout for directly accessing PXI features on system modules.

Peripheral Module

RULE: The following signals SHALL meet all the requirements of the PICMG 2.0 R3.0 specification for the 64-bit CompactPCI pinout on the peripheral slots: GND, V(I/O), AD[32:63], PAR64, C/BE[4:7]#, GA0-GA4, and UNC.

OBSERVATION: The PXI implementation of back-panel I/O uses the pins that are BRSV, CLK[1:6], GNT[1:6]#, REQ[1:6]#, and RSV in the CompactPCI 64-bit pinout for instrumentation features on peripheral modules. Note that the CLK[1:6], GNT[1:6]# and REQ[1:6]# signals are not implemented on CompactPCI peripheral modules and slots.

Backplane

RULE: The following signals SHALL meet all the requirements of the PICMG 2.0 R3.0 specification for the 64-bit CompactPCI pinout on the backplane: GND, V(I/O), AD[32:63], PAR64, C/BE[4:7]#, DEG#, FAL#, and PRST#, SYSEN#, UNC, GA0-GA4, SMB_ALERT#, SMB_SCL, SMB_SDA, and the RSV pins.

RULE: As in the CompactPCI specification, the backplane SHALL route CLK[1:6], GNT[1:6]#, and REQ[1:6]# from the system slot to the appropriate pins of the J1 connectors on the peripheral slots.

RULE: The backplane SHALL leave all the RSV lines on the system slot disconnected.

OBSERVATION: The PXI implementation of back-panel I/O uses the pins that are BRSV, CLK[1:6], GNT[1:6]#, REQ[1:6]#, and RSV (reserved) on peripheral slots and the BRSV pins on the system slot in the CompactPCI 64-bit pinout for instrumentation features on the backplane. The CLK[1:6], GNT[1:6]# and REQ[1:6]# signals are not implemented on CompactPCI backplane peripheral slots.

OBSERVATION: The PXI implementation of back-panel I/O routes all of the bused reserved signals from the CompactPCI 64-bit pinout as bused signals on the PXI backplane. However, most of the signals are not reserved in the PXI signal definition and are explained in the Section 4.1.2.5, *Trigger Bus*.

4.1.2.2 PXI Bused Reserved Signals

System Slot

The following signals are reserved for future PXI use: PXI_BRSVA15 and PXI_BRSVB4.

RULE: A system controller module SHALL NOT connect to the PXI_BRSV signals.

Peripheral Slots

The following signals are reserved for PXI use: PXI_BRSVA15 and PXI_BRSVB4.

RULE: A peripheral module SHALL NOT connect to the PXI_BRSV signals.

Backplane

The following signals are reserved for PXI use: PXI_BRSVA15 and PXI_BRSVB4.

RULE: A backplane SHALL bus each PXI_BRSV signal to each slot.

OBSERVATION: PXI_BRSV signals are implemented on the backplane exactly like CompactPCI BRSV signals.

4.1.2.3 Local Buses

PXI implements a daisy-chained local bus between adjacent peripheral modules. The local bus is a user-definable bus (13 lines wide) that can be used for a wide variety of applications. The range of applications may vary from passing an analog signal between two modules to high-speed data movement that does not affect the PXI bandwidth. For most slots, the functionality of the local bus is user-definable; however, there are specific implementations that the PXI Hardware Specification defines.

Note that the system controller module does not implement the local bus as it uses those pins for PCI arbitration and clocking functionality. The slot adjacent to the system slot uses its available local bus left signals for the star trigger functionality defined later. Similarly, the rightmost slot of the bus has no slot to its right; hence, the local bus right pins can either be unused or routed for a chassis-specific implementation. One example of chassis-specific implementation is routing the local bus to another adjacent PXI bus segment. The remainder of the slots can use the local bus for any specified purpose. Refer to Figure 2-5 for a diagram of local bus routing.

The following rules apply to all implementations of the local bus:

Peripheral Module

RULE: A peripheral module SHALL NOT drive more than ± 42 V onto any local bus line.

RULE: A peripheral module SHALL NOT drive more than 200 mA DC current into any local bus line.

PERMISSION: A peripheral module MAY connect its local bus left to its local bus right if passing the local bus to an additional module is required. This connection should be performed with caution because the length and/or characteristic impedance specifications of the local bus might be violated.

PERMISSION: On a peripheral module, a local bus signal MAY be connected to ground.

OBSERVATION: The preceding permission allows local bus implementations to have improved grounding and/or shielding.

RULE: On a peripheral module, if a local bus signal is not connected to ground, it SHALL power up in a high-impedance state. All local bus signals (except grounded ones) SHALL remain in a high-impedance state until system configuration software has determined that the local bus signals are compatible with the chassis and other peripheral modules in the system.

PERMISSION: A peripheral module MAY pull-up a local bus signal to V (I/O) to prevent an input from powering up in an unstable state.

RULE: Each peripheral module SHALL have a maximum input leakage current of 100 µA on each local bus line.

Backplane

RULE: On each bus segment, a backplane SHALL route PXI_LBR[0:12] from each slot in column A of Table 4-1 to the PXI_LBL[0:12] of the corresponding slot in column B, provided that both slots exist on the bus segment.

Table 4-1. Local Bus Routings

A	B
IDSEL = AD31	IDSEL = AD30
IDSEL = AD30	IDSEL = AD29
IDSEL = AD29	IDSEL = AD28
IDSEL = AD28	IDSEL = AD27
IDSEL = AD27	IDSEL = AD26
IDSEL = AD26	IDSEL = AD25

OBSERVATION: If a slot does not exist on the bus segment due to the AD[25:31] being used for the IDSEL of a backplane PCI device or a PCI-PCI bridge, then other local bus routings are possible provided only physically adjacent slots are connected.

OBSERVATION: There is no local bus connection to the system slot.

RULE: The backplane SHALL NOT provide any termination or buffering of local bus signals. Each signal SHALL be implemented as a direct connection between adjacent peripheral slots.

RULE: The signal length of local bus signals between slots SHALL be less than 3 in. and SHALL be matched within 1 in. between all local bus traces. The characteristic impedance of each trace SHALL be 65 Ω±10%.

PERMISSION: The backplane MAY route the local bus between two bus segments provided the signal length rule is met.

RULE: Bus segment boundaries SHALL be documented.

OBSERVATION: Documenting bus segment boundaries allows users to optimize systems by grouping boards that frequently talk to each other on the same segment.

PERMISSION: A slot at the end of a PXI segment or next to the system slot has one local bus that is not routed to another peripheral slot. The backplane MAY route these local buses for other uses.

RULE: A star trigger slot SHALL NOT implement a local bus left. Instead, the remaining pins SHALL be routed to support the star triggers.

RULE: If a chassis implements an external backplane interface with the local bus right of a slot at the end of a PXI segment, it SHALL be the highest numbered slot in the chassis.

OBSERVATION: A chassis will have at most one slot with an external backplane interface.

4.1.2.4 Reference Clock: PXI_CLK10

The PXI backplane is responsible for providing a common reference clock for synchronization of multiple modules in a measurement or control system. The variable frequency of the PCI system clock limits its usefulness in this application. PXI_CLK10 is a 10 MHz clock provided independently to each peripheral slot. PXI_CLK10 can be used to run multiple modules in synchronization from a common reference. The low skew qualities make it ideal for qualifying trigger protocols.

Backplane

RULE: The PXI_CLK10 provided by the backplane SHALL be a 10 MHz TTL signal. Its accuracy SHALL be ±100 ppm or better over the specified operating temperature and time.

OBSERVATION: Because of drift over time, the oscillator chosen MAY need to be 50 ppm accurate or better to meet the requirement of the preceding rule.

RULE: The PXI_CLK10 signal SHALL have a 50% ±5% duty cycle when measured at the 2.0 V transition point.

RULE: The clock to each peripheral slot SHALL be driven by an independent buffer that has a source impedance matched to the backplane.

RULE: The backplane SHALL provide for a skew of less than 1 ns between slots.

RECOMMENDATION: The use of low cost PLL buffers for driving the clock to each slot may lead to excessive jitter and therefore SHOULD NOT be used.

RECOMMENDATION: A backplane SHOULD allow PXI_CLK10 to be derived from an external source to allow for a more accurate reference.

OBSERVATION: The star trigger slot has defined a pin, called PXI_CLK10_IN, for providing an external clock.

RULE: If a backplane allows PXI_CLK10 to be derived from an external source, then the backplane SHALL have a 1.5K Ohm ±5% pull-down resistor on the PXI_CLK10_IN signal and receiving circuitry of this signal on the backplane SHALL be TTL compatible and 5V tolerant.

RULE: If the PXI_CLK10 is switched between sources, the minimum pulse width created SHALL be no less than 30 ns and the minimum time between successive edges of the same polarity SHALL be no less than 80 ns.

OBSERVATION: The preceding rule is intended to prevent a state machine from being corrupted by glitches in the clock during transition.

OBSERVATION: One implementation of a circuit for transitioning between sources could have the ability to select between external source, internal oscillator, and a pull-up to feed the input of a fanout buffer. The circuitry would perform the following steps in order:

1. Detect the external source.
2. Enable the pull up resistor while the internal clock is in the high state.

3. Disable the internal oscillator while in a subsequent high state.
4. Enable the external source while it is in a high state.
5. Disable the pull-up resistor in a subsequent high state of the external source.

Peripheral

RULE: Peripheral modules' PXI_CLK10 receivers SHALL be 5V tolerant.

4.1.2.5 Trigger Bus

The PXI trigger bus provides intermodule synchronization and communication. The trigger bus lines can be used for trigger or clock transmission. A few standard triggering protocols are defined to facilitate interoperability, but use of the trigger bus is not limited to the defined protocols. The PXI trigger bus lines may be used as general purpose intermodule bused lines using other manufacturer-defined protocols.

The PXI trigger bus consists of the following eight signals: PXI_TRIG[0:7]

Clock Transmission

Variable frequency clock transmission allows multiple modules to share a timebase that is not a derivative of the PXI_CLK10. For example, two data acquisition modules using a 44.1 kS/s CD audio sampling rate could share a clock that is a multiple of the 44.1 kHz. Type A drivers, defined later, prevent degradation of the clock jitter over the bused transmission medium.

PERMISSION: PXI_TRIG[0:7] MAY be used for variable frequency clock transmission.

RECOMMENDATION: To facilitate interoperability between sources and receivers of a variable frequency clock, PXI_TRIG[7] SHOULD be used to source and receive such clocks.

PXI Trigger Protocols

Some standard protocols are defined in the following sections.

PXI Asynchronous Trigger

The PXI asynchronous trigger protocol is a single-line broadcast trigger. Figure 4-1 and Table 4-2 show the timing parameters.

RULE: A PXI asynchronous trigger source SHALL meet the timing requirements listed in Table 4-2.

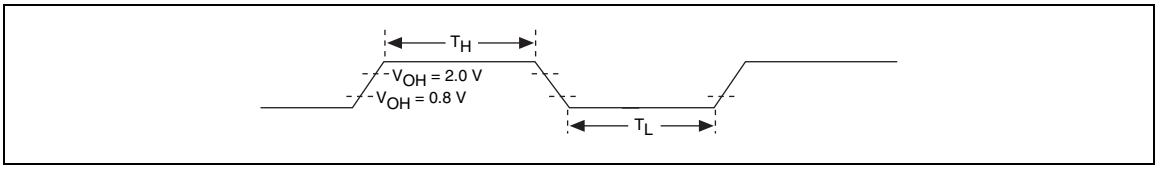

Figure 4-1. PXI Asynchronous Trigger Timing

Table 4-2. PXI Asynchronous Trigger Timing Parameters

Symbol	Parameter	Min	Max
T_h	pulse width high	18 ns	—
T_l	pulse width low	18 ns	—
Note: The pulse width is measured at the driver with a 50 pf equivalent load.			

OBSERVATION: The preceding rule guarantees PXI asynchronous trigger receivers a minimum of 10 ns pulse widths on PXI asynchronous trigger pulses.

PXI Synchronous Trigger

The PXI synchronous trigger protocol can be used to synchronize PXI_CLK10 derived timed operations on module clusters. A PXI_TRIG line is driven by a module and the participating modules respond to this line synchronously at the next PXI_CLK10 rising edge. The reference clock is PXI_CLK10.

Figure 4-2 shows PXI synchronous trigger timing.

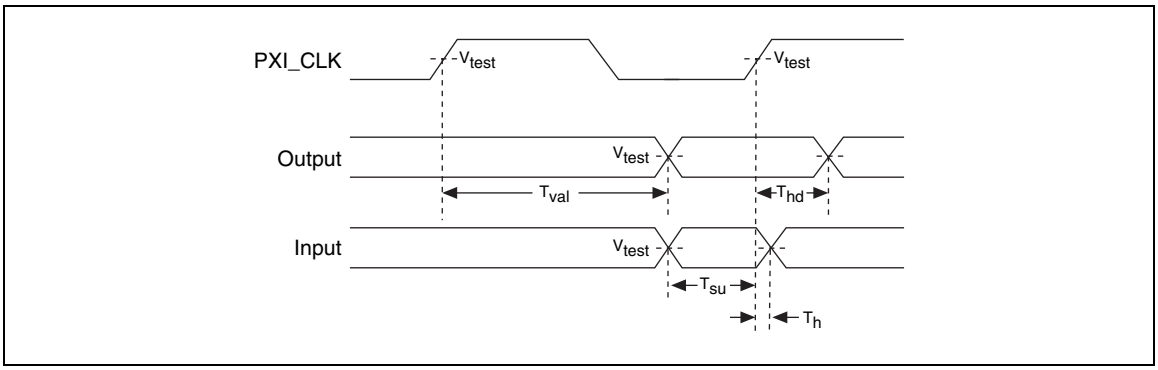

Figure 4-2. Synchronous Trigger Timing

RULE: A PXI synchronous trigger source SHALL meet the timing requirements listed in Table 4-3.

Table 4-3 lists PXI synchronous trigger timing requirements.

Table 4-3. PXI Synchronous Trigger Timing

Symbol	Parameter	Min	Max
T_{hd}	Output hold time from PXI_CLK10	2 ns	—
T_{val}	Output signal valid from PXI_CLK10	—	65 ns
T_{su}	Input set up time to PXI_CLK10	23 ns	—
T_h	Input hold time from PXI_CLK10	0 ns	—
Note: Minimum times are measured with 0 pf equivalent load. Maximum times are measured with 50 pf equivalent load.			

OBSERVATION: The output signal valid timing from PXI_CLK10 allows either rising or falling edges of PXI_CLK10 to be used for sourcing PXI synchronous triggers.

Backplane

RULE: For each PXI segment in a PXI chassis, the PXI chassis SHALL bus the PXI_TRIG[0:7] signal to each PXI slot (system and peripheral) in that segment. A chassis SHALL NOT directly connect PXI_TRIG buses from different PXI segments. If a system slot controls multiple PXI segments, it SHALL NOT directly connect PXI trigger buses from different segments.

OBSERVATION: Trigger buses from multiple segments are physically disconnected to maintain signal integrity and allow for incident wave switching of Type A trigger drivers. However, the buses may be logically connected by buffering the signals between segments.

RULE: A PXI chassis that logically connects trigger bus segments SHALL use eight bi-directional buffers to connect each trigger line of one segment to the matching trigger line on the other segment. Each buffer SHALL be able to individually route either direction between the two segments and SHALL be able to be individually tri-stated.

RULE: Buffers used for connecting trigger segments SHALL meet the same electrical requirements listed in this section for module triggers.

RULE: PXI_TRIG[0:7] SHALL be fast Schottky diode terminated at both ends of the bus segment on the backplane to + 5 V and ground as shown in Figure 4-3.

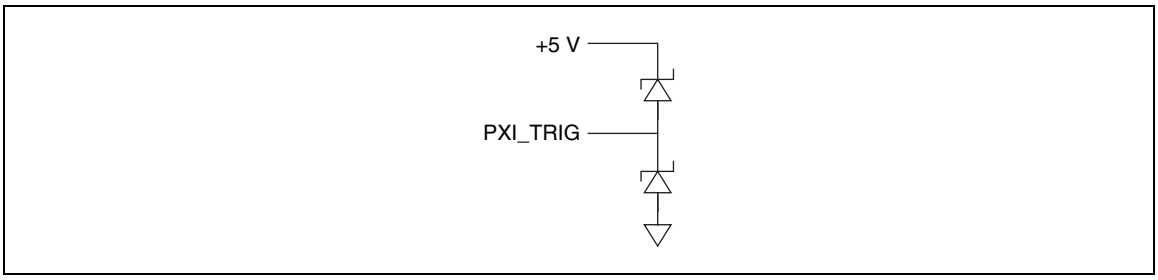

Figure 4-3. PXI Trigger Bus Termination

RULE: The *unloaded* characteristic impedance for the backplane $Z_{l,min}$ SHALL be 75 Ω ± 10% using a stripline transmission line geometry.

OBSERVATION: The higher backplane impedance lowers the driver strength requirements for incident wave switching.

RULE: The signal trace lengths of PXI trigger bus signals SHALL be less than 10 in. and matched within 1 in. between all trigger bus signals.

Peripheral or System Module

RULE: Printed circuit board trace lengths for PXI trigger bus signals SHALL be less than or equal to 1.5 in.

RECOMMENDATION: A PXI module sourcing or receiving a trigger SHOULD connect to all eight triggers and allow any of the eight triggers to be used for the sourcing or receiving functionality.

PERMISSION: A PXI module (system or peripheral) MAY leave any number of PXI trigger bus signals unconnected.

RECOMMENDATION: The following recommendations improve interoperability between modules using the PXI trigger bus. For triggering applications, if a PXI module (system or peripheral) connects to a subset of the PXI trigger signals, it SHOULD connect to PXI_STAR and PXI_TRIG[0:*n*-2] where *n* is the number of trigger lines on the peripheral module. For sourcing or receiving clocks, PXI_TRIG[7] SHOULD be used.

RULE: Upon power up, the PXI_TRIG[0:7] lines and drivers SHALL remain in a high impedance state until configured by software.

RULE: PXI_TRIG[0:7] I/O buffers SHALL be compliant with the DC specifications listed in Table 4-4.

Table 4-4. DC Specifications

Symbol	Parameter	Condition	Min	Max	Notes
Vih	Input High Voltage	—	2.0 V	Vcc + 0.5 V	[1]
Vil	Input Low Voltage	—	-0.5 V	0.8 V	—
Il	Leakage Current	0 < Vin < Vcc	—	± 70 µA	[1, 2]
Voh	Output High Voltage	Iout = - 2 mA	2.4 V	Vcc + 0.5 V	[1]
Vol	Output Low Voltage	Iout = 4 mA	-0.5 V	0.55 V	—
Cpin	Input, Output, Bidirectional Pin Capacitance	—	—	10 pf	—

Notes:
[1] Vcc refers to the 5 V power supply rail.
[2] Leakage current includes output leakage for bidirectional buffers in a high-impedance state.

OBSERVATION: The DC specifications are met by 5 V tolerant LVTTL-compatible I/O buffers.

PERMISSION: To prevent floating inputs, PXI_TRIG[0:7] lines used on a PXI module (system or peripheral) MAY be pulled up on the module with a pull-up resistance whose value is shown in Table 4-5.

Table 4-5. Pull-Up Resistor Values

Signaling Rail	Rmin	Rmax
5 V	11 kΩ	[Vccmin - Vx]/[Iih]*
3.3 V	19 kΩ	[Vccmin - Vx]/[Iih]*

* Vx = 2.4 V, which is the desired voltage on the bus in a non-driven state, and Iih is the maximum leakage current for the device buffer.

RECOMMENDATION: Type A drivers SHOULD be used for clock transmission over the PXI trigger bus. Type A drivers are capable of incident wave switching on rising edges, preventing jitter degradation due to transmission line effects. Refer to Table 4-6 for Type A driver specifications.

Table 4-6. Type A, High Current Driver, AC Specifications

Symbol	Parameter	Condition	Min	Max
Vsoh(AC)	Switching voltage high		2.3 V	—
Ioh(AC)	High source current	@Vsoh(AC)	75 mA	—

RECOMMENDATION: Intermediate voltage levels (Vol ≤V ≤Voh) may be present on the trigger bus. Schmitt trigger inputs SHOULD be used to guard against sensing multiple transitions on edge-sensitive inputs when the voltage on the bus is at intermediate levels due to transmission line effects on the bus.

RECOMMENDATION: Rising edges SHOULD be used as active edges in asynchronous trigger protocols.

4.1.2.6 Star Trigger

In addition to the bused PXI triggers, the PXI bus has included an independent trigger (PXI_STAR) for each slot that is oriented in a star configuration from the star trigger slot. The star trigger slot is adjacent to the system slot and uses the 13 left local bus signals as the star triggers. This allows a single star trigger slot to control or monitor triggers in two PCI bus segments. In systems with more than two PCI segments, it is recommended that the star triggers are only routed to the slots in the first two segments, but other routings are allowed.

The PXI Hardware Specification does not specify the functionality of the star trigger slot module or even require that the system be constructed with a star trigger module. Typical uses would include triggering multiple modules independently with low skew, monitoring a trigger from peripheral slots, and routing triggers between slots. One star trigger slot pin is dedicated to allow an external 10 MHz frequency standard to be routed as PXI_CLK10.

Backplane

RULE: The first slot to the right of the system slot in a chassis SHALL be a star trigger slot.

RULE: A chassis SHALL NOT have more than one star trigger slot.

OBSERVATION: The star trigger slot may also be used as a generic peripheral slot with the exception that the left side local bus is unavailable because these pins connect to the star triggers. The star trigger slot does not have a PXI_STAR; instead, the pin in the star trigger slot is used for an external frequency reference.

RULE: The PXI backplane SHALL route the signals from the star trigger slot to each peripheral with a trace impedance of 65 Ω±10%.

RECOMMENDATION: The PXI backplane SHOULD route the signals from the star trigger slot to each peripheral slot according to Table 4-7.

RULE: If signal routing used from the star trigger to each peripheral slot is other than that routing described in Table 4-7, or if the chassis has been designed for configurable routing, then the chassis vendor SHALL document the possible routings of such a system.

RECOMMENDATION: If the chassis has been designed for configurable routing, then the chassis vendor SHOULD provide software that can be used in all PXI frameworks to allow the user or system integrator to change the routing.

Table 4-7. Star Trigger Mapping

Star Trigger Signal	Physical Peripheral Slot
PXI_STAR0	3
PXI_STAR1	4
PXI_STAR2	5
PXI_STAR3	6
PXI_STAR4	7
PXI_STAR5	8
PXI_STAR6	9
PXI_STAR7	10

Table 4-7. Star Trigger Mapping (Continued)

Star Trigger Signal	Physical Peripheral Slot
PXI_STAR8	11
PXI_STAR9	12
PXI_STAR10	13
PXI_STAR11	14
PXI_STAR12	15

RULE: The PXI_STAR line lengths SHALL be matched in propagation delay to within 1 ns, and the delay from the star trigger slot to each peripheral module SHALL NOT exceed 5 ns.

Peripheral Module

RULE: The driver of PXI_STAR, which may be the star trigger module or a peripheral module, SHALL have a source impedance of 65 Ω±10% to match the backplane impedance.

RULE: When a peripheral module or star trigger controller drives a PXI_STAR, the signaling levels SHALL NOT exceed 5 V.

RULE: A peripheral module SHALL NOT drive its PXI_STAR when reset.

PERMISSION: A peripheral module MAY pull-up the PXI_STAR signal to prevent an unstable input.

RULE: If a peripheral module pulls up the PXI_STAR signal, the pull-up resistor SHALL be 20K Ohm or greater.

RULE: The leakage current of a peripheral module connected to PXI_STAR SHALL NOT exceed 650 µA.

OBSERVATION: The same trigger protocols defined for the PXI TTL trigger bus MAY be used on the PXI_STAR signals.

PERMISSION: The PXI_CLK10_IN signal of the star trigger slot MAY be used to provide an external 10 MHz reference for PXI_CLK10.

RULE: A module in the star trigger slot SHALL NOT drive the PXI_STAR/CLK10_IN signal, except to provide a reference for PXI_CLK10.

RULE: If a module when used in a star trigger slot can source an external 10 MHz reference onto the PXI_CLK10_IN pin, then the module SHALL only disable the external 10MHz reference while it is in a low state and the signal SHALL be tri-stated or driven low at that time.

OBSERVATION: The presence of a periodic signal on the PXI_CLK10_IN signal MAY be used to indicate that an external reference is to be used.

4.1.3 Electrical Guidelines for 6U

Larger 6U size modules are desirable for the extra module space and possibly for future additional functionality that can be provided through the J3 connector. In many cases, the extra space on a 6U module is needed only for extra circuitry, and the module requires only the J1 and J2 connectors for PXI. J3 is reserved for future revisions of the PXI Hardware Specification. This section includes the rule for connector population for 6U modules.

In an effort to make efficient use of 3U PXI modules in 6U PXI chassis, the PXI Hardware Specification defines a 6U slot that allows 3U modules to be stacked within. This allows two 3U modules to be used in 1 6U slot. These systems have P4 and P5 populated in the slots that support stacking 3U modules. P4 and P5 will be routed as if they were another segment of the PXI backplane. This section also covers the electrical rules associated with 6U PXI chassis which support this feature and defines a 6U Star Trigger Controller that can synchronize star triggers going to 3U modules that are stacked in a 6U slot.

4.1.3.1 6U Peripheral Module Connector Population

RULE: 6U PXI peripheral modules that are not 6U star trigger controllers SHALL implement only J1 and J2. J3 SHALL NOT be loaded on 6U peripheral modules.

PERMISSION: Since J5 is not reserved for future revisions of the PXI Hardware Specification, vendors MAY use J5 for custom implementations of PXI provided they only offer such a module as part of their custom PXI system.

4.1.3.2 6U Chassis that Support Stacking 3U Modules

RULE: 6U slots that support stacking 3U modules SHALL populate P4 and P5.

RULE*:* 6U slots that support stacking 3U modules SHALL route the signals on the P4 connector according to the rules in Sections 4.1.1, 4.1.2, and 4.2 for P1.

RULE: 6U slots that support stacking 3U modules SHALL route the signals on the P5 connector according to the rules in Sections 4.1.1, 4.1.2, and 4.2 for P2.

RULE: 6U chassis that support stacking 3U modules SHALL support stacking 3U modules in the star trigger slot.

OBSERVATION: The preceding rule ensures that up to 13 3U modules that reside in the P4/P5 position of 6U slots have their star trigger line routed to the star trigger slot.

PERMISSION: A 6U star trigger controller MAY populate J5 to allow star triggers to connect to 3U modules that have been stacked in the P4/P5 position of the 6U slot.

RULE: A 6U star trigger controller that populates J5 SHALL NOT connect to any signals on the J5 connector other than the star trigger lines and the PXI trigger bus.

RULE: If PCI to PCI bridging between the segment or segments created by the P4 and P5 connectors and the segment or segments created by the P1 and P2 connectors is needed to meet PCI bus length and loading requirements, then it SHALL be provided by the backplane and SHALL NOT be provided by the System Controller Module.

OBSERVATION: The preceding rule allows most 6U CompactPCI System Controller Modules to work in 6U PXI chassis that support stacking 3U modules.

4.2 Connector Pin Assignments (J1/P1 and J2/P2)

To help in reviewing the tables in this section and locating the appropriate specification for signal requirements, Table 4-8 lists all signals alphabetically by original specification (PXI, CompactPCI, or PCI).

Table 4-8. PXI System Signal Groups

System	Signals		
PXI	PXI_BRSV PXI_CLK10 PXI_CLK10_IN	PXI_LBL[0:12] PXI_LBR[0:12]	PXI_STAR[0:12] PXI_TRIG[0:7]
CompactPCI	BD_SEL# BRSV CLK[0:6] DEG# ENUM# FAL# GA0-GA4 GNT#[0:6]	HEALTHY# INTP INTS IPMB_PWR IPMB_SCL IPMB_SDA PRST#	REQ#[0:6] RSV SYSEN# SMB_ALERT# SMB_SCL SMB_SDA UNC
PCI	ACK64# AD[0:63] C/BE[0:7]# CLK DEVSEL# FRAME# GND GNT# IDSEL INTA# INTB# INTC#	INTD# IRDY# LOCK# M66EN PAR PAR64 PERR# REQ# REQ64# RST# SERR# STOP#	TCK TDI TDO TMS TRDY# TRST# V(I/O) 3.3 V 5 V +12 V -12 V

4.2.1 General Peripheral Slots

Table 4-9 gives the peripheral slot pinout for the J1 and J2 connector. PXI-specific signals are shown in **bold**.

RULE: Peripheral modules and backplane peripheral slots SHALL use the pinout in Table 4-9.

Table 4-9. Generic Peripheral Slot Pinout

22	GND	GA4	GA3	GA2	GA1	GA0	GND	P2/J2 CONNECTOR
21	GND	**PXI_LBR0**	RSV	**PXI_LBR1**	**PXI_LBR2**	**PXI_LBR3**	GND	
20	GND	**PXI_LBR4**	**PXI_LBR5**	**PXI_LBL0**	GND	**PXI_LBL1**	GND	
19	GND	**PXI_LBL2**	RSV	**PXI_LBL3**	**PXI_LBL4**	**PXI_LBL5**	GND	
18	GND	**PXI_TRIG3**	**PXI_TRIG4**	**PXI_TRIG5**	GND	**PXI_TRIG6**	GND	
17	GND	**PXI_TRIG2**	GND	RSV	**PXI_STAR**	**PXI_CLK10**	GND	
16	GND	**PXI_TRIG1**	**PXI_TRIG0**	RSV	GND	**PXI_TRIG7**	GND	
15	GND	**PXI_BRSVA15**	GND	RSV	**PXI_LBL6**	**PXI_LBR6**	GND	
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND	
13	GND	AD[38]	GND	V(I/O)	AD[37]	AD[36]	GND	
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND	
11	GND	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND	
10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND	
9	GND	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND	
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND	
7	GND	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND	
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND	
5	GND	C/BE[5]#	GND	V(I/O)	C/BE[4]#	PAR64	GND	
4	GND	V(I/O)	**PXI_BRSVB4**	C/BE[7]#	GND	C/BE[6]#	GND	
3	GND	**PXI_LBR7**	GND	**PXI_LBR8**	**PXI_LBR9**	**PXI_LBR10**	GND	
2	GND	**PXI_LBR11**	**PXI_LBR12**	UNC	**PXI_LBL7**	**PXI_LBL8**	GND	
1	GND	**PXI_LBL9**	GND	**PXI_LBL10**	**PXI_LBL11**	**PXI_LBL12**	GND	
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND	P1/J1 CONNECTOR
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND	
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND	
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND	
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND	
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND	
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND	
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND	
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND	
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND	
15	GND	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND	
12–14	Key Area							
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND	
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND	
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND	
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND	
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND	
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND	
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND	
4	GND	IPMB_PWR	HEALTHY#	V(I/O)	INTP	INTS	GND	
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND	
2	GND	TCK	5V	TMS	TDO	TDI	GND	
1	GND	5V	-12V	TRST#	+12V	5V	GND	
Pin	**Z**	**A**	**B**	**C**	**D**	**E**	**F**	

4.2.2 System Slot

Table 4-10 gives the system slot pinout for the J1 and J2 connectors. PXI-specific signals are shown in **bold**.

RULE: System modules and backplane system slots SHALL use the pinout in Table 4-10.

Table 4-10. System Slot Pinout

22	GND	GA4	GA3	GA2	GA1	GA0	GND	P2/J2 CONNECTOR
21	GND	CLK6	GND	RSV	RSV	RSV	GND	
20	GND	CLK5	GND	RSV	GND	RSV	GND	
19	GND	GND	GND	SMB_SDA	SMB_SCL	SMB_ALERT#	GND	
18	GND	**PXI_TRIG3**	**PXI_TRIG4**	**PXI_TRIG5**	GND	**PXI_TRIG6**	GND	
17	GND	**PXI_TRIG2**	GND	PRST#	REQ6#	GNT6#	GND	
16	GND	**PXI_TRIG1**	**PXI_TRIG0**	DEG#	GND	**PXI_TRIG7**	GND	
15	GND	**PXI_BRSVA15**	GND	FAL#	REQ5#	GNT5#	GND	
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND	
13	GND	AD[38]	GND	V(I/O)	AD[37]	AD[36]	GND	
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND	
11	GND	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND	
10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND	
9	GND	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND	
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND	
7	GND	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND	
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND	
5	GND	C/BE[5]#	GND	V(I/O)	C/BE[4]#	PAR64	GND	
4	GND	V(I/O)	**PXI_BRSVB4**	C/BE[7]#	GND	C/BE[6]#	GND	
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND	
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND	
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND	
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND	P1/J1 CONNECTOR
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND	
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND	
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND	
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND	
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND	
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND	
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND	
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND	
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND	
15	GND	3.3V	FRAME#	IRDY#	GND	TRDY#	GND	
12–14	Key Area							
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND	
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND	
9	GND	C/BE[3]#	GND	AD[23]	GND	AD[22]	GND	
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND	
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND	
6	GND	REQ0#	GND	3.3V	CLK0	AD[31]	GND	
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT0#	GND	
4	GND	IPMB_PWR	HEALTHY#	V(I/O)	INTP	INTS	GND	
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND	
2	GND	TCK	5V	TMS	TDO	TDI	GND	
1	GND	5V	-12V	TRST#	+12V	5V	GND	
Pin	**Z**	**A**	**B**	**C**	**D**	**E**	**F**	

4.2.3 Star Trigger Slot

Table 4-11 gives the peripheral slot pinout for the J1 and J2 connectors of the star trigger slot. PXI-specific signals are shown in **bold**.

RULE: Star trigger modules and backplane star trigger slots SHALL use the pinout in Table 4-11.

Table 4-11. Star Trigger Slot Pinout

22	GND	GA4	GA3	GA2	GA1	GA0	GND	P2/J2 CONNECTOR
21	GND	**PXI_LBR0**	RSV	**PXI_LBR1**	**PXI_LBR2**	**PXI_LBR3**	GND	
20	GND	**PXI_LBR4**	**PXI_LBR5**	**PXI_STAR0**	GND	**PXI_STAR1**	GND	
19	GND	**PXI_STAR2**	RSV	**PXI_STAR3**	**PXI_STAR4**	**PXI_STAR5**	GND	
18	GND	**PXI_TRIG3**	**PXI_TRIG4**	**PXI_TRIG5**	GND	**PXI_TRIG6**	GND	
17	GND	**PXI_TRIG2**	GND	RSV	**PXI_CLK10_IN**	**PXI_CLK10**	GND	
16	GND	**PXI_TRIG1**	**PXI_TRIG0**	RSV	GND	**PXI_TRIG7**	GND	
15	GND	**PXI_BRSVA15**	GND	RSV	**PXI_STAR6**	**PXI_LBR6**	GND	
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND	
13	GND	AD[38]	GND	V(I/O)	AD[37]	AD[36]	GND	
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND	
11	GND	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND	
10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND	
9	GND	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND	
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND	
7	GND	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND	
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND	
5	GND	C/BE[5]#	GND	V(I/O)	C/BE[4]#	PAR64	GND	
4	GND	V(I/O)	**PXI_BRSVB4**	C/BE[7]#	GND	C/BE[6]#	GND	
3	GND	**PXI_LBR7**	GND	**PXI_LBR8**	**PXI_LBR9**	**PXI_LBR10**	GND	
2	GND	**PXI_LBR11**	**PXI_LBR12**	UNC	**PXI_STAR7**	**PXI_STAR8**	GND	
1	GND	**PXI_STAR9**	GND	**PXI_STAR10**	**PXI_STAR11**	**PXI_STAR12**	GND	
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND	P1/J1 CONNECTOR
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND	
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND	
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND	
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND	
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND	
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND	
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND	
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND	
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND	
15	GND	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND	
12–14	Key Area							
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND	
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND	
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND	
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND	
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND	
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND	
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND	
4	GND	IPMB_PWR	HEALTHY#	V(I/O)	INTP	INTS	GND	
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND	
2	GND	TCK	5V	TMS	TDO	TDI	GND	
1	GND	5V	-12V	TRST#	+12V	5V	GND	
Pin	**Z**	**A**	**B**	**C**	**D**	**E**	**F**	

4.3 Chassis Power Supply Specifications

Minimum power supply requirements are specified to ensure that module designers can design modules knowing that they will operate in any PXI system. The PXI Power requirements specified in this section apply to any PXI chassis regardless of the number of slots or form-factor (3U or 6U).

RULE: The power supply in a PXI chassis SHALL provide at least the required amounts of current specified in Table 4-12.

RULE: 6U Slots that support stacking 3U modules SHALL be considered two slots when determining the amount of current required of the power supply.

Table 4-12. PXI Chassis Power Supply Minimum Power Requirements

	5 V		3.3 V		+12 V	-12 V
	System Slot	**Each Peripheral Slot**	**System Slot**	**Each Peripheral Slot**	**All Slots**	**All Slots**
Required Current	6 A	2 A	6 A	2A	0.5 A	0.25 A

OBSERVATION: The minimum current for each voltage rail provided by a power supply in a PXI Chassis with N slots can be determined by the following formulas:

5V: $6A + (N - 1) \times 2A$

3.3V: $6A + (N - 1) \times 2A$

+12V: $N \times 0.5A$

-12V: $N \times 0.25A$

For an 8-slot chassis, the minimum current for each voltage rail for the entire chassis would be as follows:

5V: $6A \text{ (system)} + 2A \times 7 \text{ (peripheral)} = 20A$

3.3V: $6A \text{ (system)} + 2A \times 7 \text{ (peripheral)} = 20A$

+12V: $0.5A \times 8 \text{ (all slots)} = 4A$

-12V: $0.25 \times 8 \text{ (all slots)} = 2A$

For a 14-slot chassis, the minimum current for each voltage rail for the entire chassis would be as follows:

5V: $6A \text{ (system)} + 2A \times 13 \text{ (peripheral)} = 32A$

3.3V: $6A \text{ (system)} + 2A \times 13 \text{ (peripheral)} = 32A$

+12V: $0.5A \times 14 \text{ (all slots)} = 7A$

-12V: $0.25 \times 14 \text{ (all slots)} = 3.5A$

OBSERVATION: The minimum power provided by a power supply in a PXI Chassis with N slots is equivalent to the formula:

$5V \times (6A + (N - 1) \times 2A) + 3.3V \times (6A + (N - 1) \times 2A) + 12V \times (N \times 0.5A) + 12V \times (N \times 0.25A)$

PERMISSION: Power Supplies MAY provide additional current beyond the required amounts specified in Table 4-12.

OBSERVATION: Having the system supply 3.3 V conserves space and heat in the system slot module because 5 V does not have to be converted to 3.3 V on the module.

OBSERVATION: Each generation of processors requires more power than the previous generation. Providing copious amounts of power and cooling to the system slot of a chassis can extend the product applicability in the future.

RULE: All modules SHALL document and make available to the customer their current requirements to allow users to maximize the capabilities of their power supply.

RULE: The power distribution mechanism of a backplane in a PXI chassis SHALL be capable of providing the amounts of current specified in Table 4-13 to each slot.

Table 4-13. Minimum Current Handling Per Slot

5 V	3.3 V	+12V	-12V
6A	6A	1A	1A

OBSERVATION: The power supply of a PXI chassis is not required to supply the current listed in Table 4-13 to all slots simultaneously. Overall current per rail supplied by a power supply to all slots is not required to be greater than the minimum power requirements specified in Table 4-12.

RULE: A peripheral or system slot module SHALL NOT draw more than 1 A of current from any power pin or return more than 1 A of current through any ground pin.

4.3.1 Low Power Chassis Power Supply Specifications

A chassis designed for portable applications or one with a DC power input may be constrained by the battery and operating hours. This may make meeting the minimum power requirements listed in Table 4-12 impractical, but minimum power requirements for this class of chassis are still important for interoperability with modules. The minimum power requirements for low power chassis are set to allow at least one system controller and two peripheral modules to work in the chassis, regardless of 3U/6U or the number of slots available.

PERMISSION: A low power PXI chassis MAY have less power than is required in Table 4-12.

RULE: A low power PXI chassis that has less power than is required in Table 4-12 input SHALL provide at least the required amounts of current specified in Table 4-14.

Table 4-14. Low Power PXI Chassis Power Supply Minimum Power Requirements

	5 V		3.3 V		+12 V	-12 V
	System Slot 6 A	Each Peripheral Slot 2 A	System Slot 6 A	Each Peripheral Slot 2 A	Each Slot 0.5 A	Each Slot 0.25 A
Total Required Current	10 A		10 A		1.5 A	0.75 A

RULE: PXI chassis having less power than is required in Table 4-12 and meet the requirements in Table 4-14 SHALL have the text LOW POWER clearly visible with a character height of at minimum 4mm on the front of the chassis as shown in Figure 4-4. Logo artwork can be obtained from the PXI Systems Alliance.

LOW POWER

Figure 4-4. Text Required for Low Power Chassis

4.4 PXI Module Ground Connections

The PXI backplane provides power and ground connections on the P1/J1 and P2/J2 connectors. The power connections will carry ripple currents introduced by the PXI chassis power supply and time varying power loads of the modules fitted. The PXI backplane grounds will have a voltage on them because of the current drawn by the modules and returned, by the module, back to the PXI power supply via the backplane.

For applications where the system is to be used to perform parametric measurements it is important to make sure that the currents flowing in the PXI backplane connections do not cause interference which results in unwanted currents or voltages on the ground of the front panel of PXI chassis, the point most commonly used as the reference in single ended outputs (such as RF applications).

An example ground arrangement is shown in Figure 4-5.

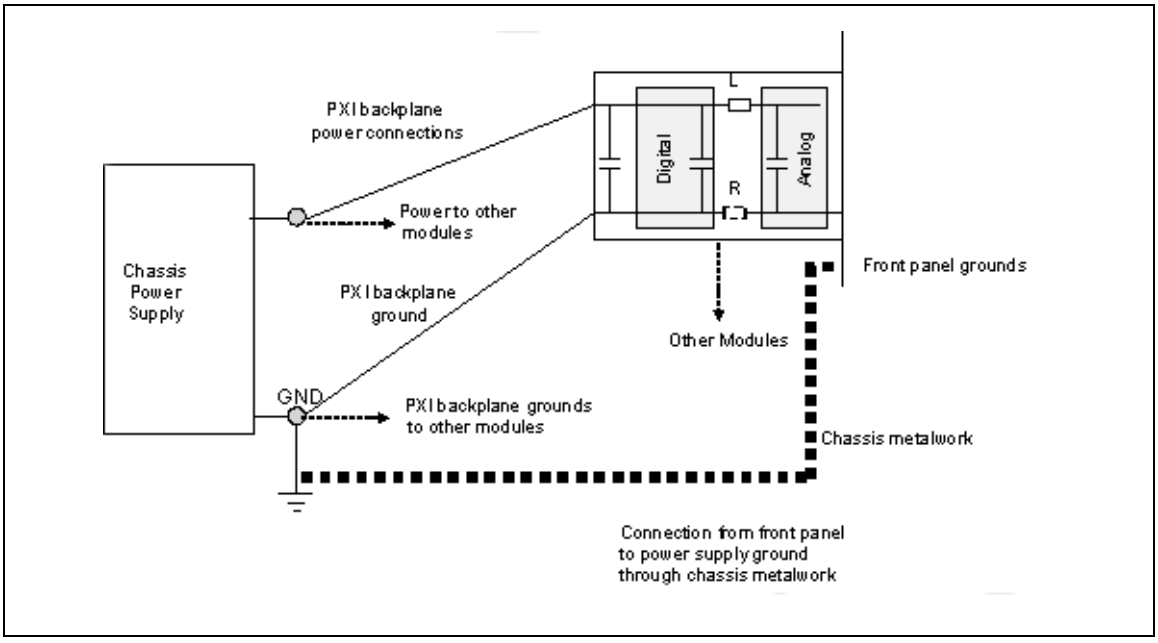

Figure 4-5. Power and Ground Connections on a PXI Module

For clarity only one module, one power supply and one ground connection is shown. In practice a number of connections are made to each module.

Power from the chassis power supply is supplied to the modules from star connection points. Where practical the AC currents flowing down the power supply lines should be returned to the power supply ground star connection.

The impedance of the connection between the front panel grounds of the modules and to the chassis power supply ground is low, but the presence of any current can generate unwanted voltages across the module front panels that will degrade a system's performance.

The level of current injected into the front panel ground can be reduced by appropriate choice of the decoupling components and the separation of digital and analog grounds, one example of which is shown in Figure 4-5.

RECOMMENDATION: Modules SHOULD be designed so that they minimize the injection of AC currents into the front panel ground of PXI modules.

RECOMMENDATION: Where possible, alternating currents SHOULD be returned to the power supply by using a suitable decoupling arrangement on the PXI power supply and returning the current to the power supply via the PXI backplane ground.

RECOMMENDATION: Where possible high speed digital circuits, and particularly the PCI interface devices, SHOULD use the PXI backplane ground in preference to the module front panel ground in order to avoid injecting AC signals into the module front panels.

RECOMMENDATION: Analog component grounds SHOULD be referenced to the module front panel ground.

RECOMMENDATION: The front panel ground and the PXI (digital) backplane ground SHOULD be separated so that the high speed clock edges do not produce spurious signals in the analog circuits. Some coupling between the two grounds is inevitable through capacitive or inductive coupling; these effects SHOULD be minimized by careful consideration of the module layout and component placement and the correct use of local decoupling capacitors for the application.

OBSERVATION: Having the front panel ground and the digital ground entirely separated may make the module unduly sensitive to static handling problems. This can be alleviated by adding a resistor between the two grounds whose value is significantly higher than the impedance of the PXI ground to the chassis power supply ground, a value of greater than 10 ohms and less than 100 k ohms being adequate is most cases. The presence of a 10 ohm connection is unlikely to introduce significant current since it is much higher than the resistance from the PXI backplane ground to the power supply.

OBSERVATION: In some modules high speed digital signals may be connected to the front panel ground in order to meet performance standards required of the module, and it may not be possible to follow all the guidelines indicated in this section of the standard.

OBSERVATION: The ground of high speed digital circuits should be returned back to the PXI ground and not the analog ground

OBSERVATION: Analog circuits should be grounded to the front panel of the module.

OBSERVATION: The front panel ground and the PXI ground can be connected together by a resistor (10 ohms or greater) to avoid static handling problems for the PXI module.

OBSERVATION: Modules should be designed to maximize the impedance above 100 kHz between the PXI backplane ground and the module front panel.

5. PXI Software Specification Compliance

Revision 2.0 and earlier of the PXI Specification included software requirements for PXI modules, chassis and systems. From PXI Hardware Specification revision 2.1 and higher, the PXI Systems Alliance maintains a separate software specification for PXI modules, chassis and systems. PXI modules, chassis, and systems developed to comply with this PXI Hardware Specification must also comply with the PXI Software Specification.

RULE: PXI modules, chassis, and systems SHALL comply with the rules defined in the PXI Software Specification maintained by the PXI Systems Alliance.

6. PXI 32-bit

Revision 2.1 and earlier of the PXI Hardware Specification required all backplanes be routed to support 64-bit PCI. Many PXI modules only require 32-bit PCI support which could be used in lower cost chassis that support 32-bit PCI only. This section defines a PXI chassis that does not support 64-bit PCI. Additionally since the upper 32-bit PCI signals will not be used in these chassis, suppliers of PXI chassis may decide to use these signals for rear I/O purposes. This allows PXI controllers to pass vendor specific signals through the backplane to support functions such as video and mass storage within or through the back of the chassis. Controllers shall be designed to isolate the rear I/O functionality on the J2 connector based on the state of the 64EN# signal. Because there is a potential for incompatibility between different controller and chassis implementations of rear I/O, chassis that support rear I/O have additional labeling and marketing requirements and controllers that support rear I/O have additional marketing requirements.

RULE: PXI chassis that don't support 64-bit PCI SHALL leave the 64EN# (J2-B5) pin unconnected.

RULE: PXI controllers that support rear I/O functionality on the upper 32-bit PCI pins on the J2 connector SHALL use 64EN# (J2-B5) to determine if the backplane supports 64-bit PCI. If 64EN# is active (low) the system controller SHALL isolate the rear I/O functionality from the BP(I/O) pins and SHALL pull-up the rear I/O pins to V(I/O) per the CompactPCI specification. If 64EN# is inactive (floating) then the system controller can enable the rear I/O functionality to the BP(I/O) pins.

RULE: PXI chasiss that support rear I/O on the upper 32-bit PCI pins (3U & 6U) or support rear I/O on the P3, P4, P5 (6U) connectors SHALL have the text REAR I/O clearly visible with a character height of at minimum 4mm on the front of the chassis as shown in Figure 6-1. Logo artwork can be obtained from the PXI Systems Alliance.

Figure 6-1. Text Required for Rear I/O Chassis

RULE: PXI system controllers that implement rear I/O functionality SHALL have the following text in their marketing information, manuals, and datasheets: *Notice: This PXI controller implements rear I/O. PXI controllers with rear I/O were designed to operate with a matching rear transition module which provides internal or external chassis I/O. Warning: If this PXI controller is used with a chassis that contains a rear transition module that does not match the controller, the rear I/O functionality may not operate and may cause damage to the PXI controller or the rear transition module.*

RULE: PXI chassis that implement rear I/O functionality SHALL have the following text in their marketing information, manuals, and datasheets: *Notice: This PXI chassis implements rear I/O. PXI chassis with rear I/O were designed to provide internal or external chassis I/O using a rear transition module that matches the PXI controller. Warning: If this PXI chassis is used with a controller that does not match the rear transition module, the rear I/O functionality may not operate and may cause damage to the PXI controller or the rear transition module.*

RULE: PXI system controllers and chassis that implement rear I/O functionality SHALL have their rear I/O pin definition documented in the product manuals.

OBSERVATION: System controller modules might only support a 32-bit PCI interface to the PXI backplane but don't implement rear I/O functionality. These controllers do not have additional requirements for their marketing information, manuals, or datasheets**.**

RULE: System controllers that implement rear I/O and backplanes that only support 32-bit PCI SHALL comply with all previous defined rules except they SHALL follow the pin definitions in Table 6-1, Table 6-2, and Table 6-3.

RULE: Backplanes that do not support 64-bit PCI SHALL leave the BP(I/O) and RSV pins unconnected.

PERMISSION: Suppliers MAY decide how to use the BP(I/O) pins on system controllers that support rear I/O.

PERMISSION: Suppliers MAY support a 50mm deep rear transition module in chassis that support 32-bit PCI only.

PERMISSION: Suppliers MAY choose how to make use of the supplier defined signals coming from the BP(I/O) pins in chassis that don't support 64-bit PCI.

6.1 32-bit PCI Only General Peripheral Slots

Table 6-1 gives the peripheral slot pinout for the P1 and P2 connector of a backplane that supports 32-bit PCI only. PXI-specific signals are shown in **bold**.

Table 6-1. 32-bit PCI Only Generic Peripheral Slot Pinout

22	GND	GA4	GA3	GA2	GA1	GA0	GND	P2/J2 CONNECTOR
21	GND	**PXI_LBR0**	RSV	**PXI_LBR1**	**PXI_LBR2**	**PXI_LBR3**	GND	
20	GND	**PXI_LBR4**	**PXI_LBR5**	**PXI_LBL0**	GND	**PXI_LBL1**	GND	
19	GND	**PXI_LBL2**	RSV	**PXI_LBL3**	**PXI_LBL4**	**PXI_LBL5**	GND	
18	GND	**PXI_TRIG3**	**PXI_TRIG4**	**PXI_TRIG5**	GND	**PXI_TRIG6**	GND	
17	GND	**PXI_TRIG2**	GND	RSV	**PXI_STAR**	**PXI_CLK10**	GND	
16	GND	**PXI_TRIG1**	**PXI_TRIG0**	RSV	GND	**PXI_TRIG7**	GND	
15	GND	**PXI_BRSVA15**	GND	RSV	**PXI_LBL6**	**PXI_LBR6**	GND	
14	GND	RSV	RSV	RSV	GND	RSV	GND	
13	GND	RSV	GND	V(I/O)	RSV	RSV	GND	
12	GND	RSV	RSV	RSV	GND	RSV	GND	
11	GND	RSV	GND	V(I/O)	RSV	RSV	GND	
10	GND	RSV	RSV	RSV	GND	RSV	GND	
9	GND	RSV	GND	V(I/O)	RSV	RSV	GND	
8	GND	RSV	RSV	RSV	GND	RSV	GND	
7	GND	RSV	GND	V(I/O)	RSV	RSV	GND	
6	GND	RSV	RSV	RSV	GND	RSV	GND	
5	GND	RSV	64EN#	V(I/O)	RSV	RSV	GND	
4	GND	V(I/O)	**PXI_BRSVB4**	RSV	GND	RSV	GND	
3	GND	**PXI_LBR7**	GND	**PXI_LBR8**	**PXI_LBR9**	**PXI_LBR10**	GND	
2	GND	**PXI_LBR11**	**PXI_LBR12**	UNC	**PXI_LBL7**	**PXI_LBL8**	GND	
1	GND	**PXI_LBL9**	GND	**PXI_LBL10**	**PXI_LBL11**	**PXI_LBL12**	GND	
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND	P1/J1 CONNECTOR
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND	
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND	
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND	
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND	
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND	
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND	
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND	
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND	
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND	
15	GND	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND	
12–14	Key Area							
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND	
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND	
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND	
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND	
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND	
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND	
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND	
4	GND	IPMB_PWR	HEALTHY#	V(I/O)	INTP	INTS	GND	
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND	
2	GND	TCK	5V	TMS	TDO	TDI	GND	
1	GND	5V	-12V	TRST#	+12V	5V	GND	
Pin	**Z**	**A**	**B**	**C**	**D**	**E**	**F**	

6.2 Rear I/O System Slot

Table 6-2 gives the system slot pinout for the P1 and P2 connector of a backplane that supports rear I/O. PXI-specific signals are shown in **bold**.

Table 6-2. Rear I/O System Slot Pinout

22	GND	GA4	GA3	GA2	GA1	GA0	GND	P2/J2 CONNECTOR
21	GND	CLK6	GND	RSV	RSV	RSV	GND	
20	GND	CLK5	GND	RSV	GND	RSV	GND	
19	GND	GND	GND	SMB_SDA	SMB_SCL	SMB_ALERT#	GND	
18	GND	**PXI_TRIG3**	**PXI_TRIG4**	**PXI_TRIG5**	GND	**PXI_TRIG6**	GND	
17	GND	**PXI_TRIG2**	GND	PRST#	REQ6#	GNT6#	GND	
16	GND	**PXI_TRIG1**	**PXI_TRIG0**	DEG#	GND	**PXI_TRIG7**	GND	
15	GND	**PXI_BRSVA15**	GND	FAL#	REQ5#	GNT5#	GND	
14	GND	BP(I/O)	BP(I/O)	BP(I/O)	GND	BP(I/O)	GND	
13	GND	BP(I/O)	GND	V(I/O)	BP(I/O)	BP(I/O)	GND	
12	GND	BP(I/O)	BP(I/O)	BP(I/O)	GND	BP(I/O)	GND	
11	GND	BP(I/O)	GND	V(I/O)	BP(I/O)	BP(I/O)	GND	
10	GND	BP(I/O)	BP(I/O)	BP(I/O)	GND	BP(I/O)	GND	
9	GND	BP(I/O)	GND	V(I/O)	BP(I/O)	BP(I/O)	GND	
8	GND	BP(I/O)	BP(I/O)	BP(I/O)	GND	BP(I/O)	GND	
7	GND	BP(I/O)	GND	V(I/O)	BP(I/O)	BP(I/O)	GND	
6	GND	BP(I/O)	BP(I/O)	BP(I/O)	GND	BP(I/O)	GND	
5	GND	BP(I/O)	64EN#	V(I/O)	BP(I/O)	BP(I/O)	GND	
4	GND	V(I/O)	**PXI_BRSVB4**	BP(I/O)	GND	BP(I/O)	GND	
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND	
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND	
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND	
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND	P1/J1 CONNECTOR
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND	
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND	
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND	
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND	
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND	
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND	
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND	
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND	
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND	
15	GND	3.3V	FRAME#	IRDY#	GND	TRDY#	GND	
12–14	Key Area							
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND	
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND	
9	GND	C/BE[3]#	GND	AD[23]	GND	AD[22]	GND	
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND	
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND	
6	GND	REQ0#	GND	3.3V	CLK0	AD[31]	GND	
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT0#	GND	
4	GND	IPMB_PWR	HEALTHY#	V(I/O)	INTP	INTS	GND	
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND	
2	GND	TCK	5V	TMS	TDO	TDI	GND	
1	GND	5V	-12V	TRST#	+12V	5V	GND	
Pin	**Z**	**A**	**B**	**C**	**D**	**E**	**F**	

6.3 32-bit PCI Only Star Trigger Slot

Table 6-3 gives the star trigger slot pinout for the P1 and P2 connector of a backplane that supports 32-bit PCI only. PXI-specific signals are shown in **bold**.

Table 6-3. 32-bit PCI Only Star Trigger Slot Pinout

22	GND	GA4	GA3	GA2	GA1	GA0	GND	P2/J2 CONNECTOR
21	GND	**PXI_LBR0**	RSV	**PXI_LBR1**	**PXI_LBR2**	**PXI_LBR3**	GND	
20	GND	**PXI_LBR4**	**PXI_LBR5**	**PXI_STAR0**	GND	**PXI_STAR1**	GND	
19	GND	**PXI_STAR2**	RSV	**PXI_STAR3**	**PXI_STAR4**	**PXI_STAR5**	GND	
18	GND	**PXI_TRIG3**	**PXI_TRIG4**	**PXI_TRIG5**	GND	**PXI_TRIG6**	GND	
17	GND	**PXI_TRIG2**	GND	RSV	**PXI_CLK10_IN**	**PXI_CLK10**	GND	
16	GND	**PXI_TRIG1**	**PXI_TRIG0**	RSV	GND	**PXI_TRIG7**	GND	
15	GND	**PXI_BRSVA15**	GND	RSV	**PXI_STAR6**	**PXI_LBR6**	GND	
14	GND	RSV	RSV	RSV	GND	RSV	GND	
13	GND	RSV	GND	V(I/O)	RSV	RSV	GND	
12	GND	RSV	RSV	RSV	GND	RSV	GND	
11	GND	RSV	GND	V(I/O)	RSV	RSV	GND	
10	GND	RSV	RSV	RSV	GND	RSV	GND	
9	GND	RSV	GND	V(I/O)	RSV	RSV	GND	
8	GND	RSV	RSV	RSV	GND	RSV	GND	
7	GND	RSV	GND	V(I/O)	RSV	RSV	GND	
6	GND	RSV	RSV	RSV	GND	RSV	GND	
5	GND	RSV	64EN#	V(I/O)	RSV	RSV	GND	
4	GND	V(I/O)	**PXI_BRSVB4**	RSV	GND	RSV	GND	
3	GND	**PXI_LBR7**	GND	**PXI_LBR8**	**PXI_LBR9**	**PXI_LBR10**	GND	
2	GND	**PXI_LBR11**	**PXI_LBR12**	UNC	**PXI_STAR7**	**PXI_STAR8**	GND	
1	GND	**PXI_STAR9**	GND	**PXI_STAR10**	**PXI_STAR11**	**PXI_STAR12**	GND	
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND	P1/J1 CONNECTOR
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND	
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND	
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND	
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND	
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND	
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND	
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND	
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND	
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND	
15	GND	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND	
12–14	Key Area							
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND	
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND	
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND	
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND	
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND	
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND	
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND	
4	GND	IPMB_PWR	HEALTHY#	V(I/O)	INTP	INTS	GND	
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND	
2	GND	TCK	5V	TMS	TDO	TDI	GND	
1	GND	5V	-12V	TRST#	+12V	5V	GND	
Pin	**Z**	**A**	**B**	**C**	**D**	**E**	**F**	