PXI™-5

PXI Express Hardware Specification

PCI EXPRESS eXtensions for Instrumentation

An Implementation of *CompactPCI® Express*

Revision 1.0
August 22, 2005

PXI Systems Alliance

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PXI Express Hardware Specification Revision History

This section is an overview of the revision history of the PXI Express Hardware Specification.

Revision 1.0, August 22, 2005

This is the first public revision of the PXI Express specification.

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1. Introduction

This section describes the primary objectives and scope of the PXI-5: PCI Express eXtensions for Instrumentation specification. It also defines the intended audience and lists relevant terminology and documents.

1.1 Objectives

PXI Express was created to build on the successful PXI-1: PXI Hardware Specification and the new CompactPCI Express standard to make new levels of performance possible in modular instrumentation and automation Systems. Similar to the PXI-1 standard, existing industry standards are leveraged by PXI Express to benefit from high component availability at lower costs. PXI Express also continues to maintain software compatibility with industry-standard personal computers, allowing customers to use the same software tools and environments with which they are familiar. Not only does PXI Express provide a giant leap in measurement and automation performance, but it also provides a high level of compatibility with PXI-1, so customers can preserve their investment in PXI-1 Modules.

PXI Express leverages the electrical features defined by the widely adopted PCI Express specification for data movement. This is accomplished by PXI Express Modules complying with the CompactPCI Express specification, which combines the PCI Express electrical specification with rugged Eurocard mechanical packaging and high-performance differential connectors. This allows measurement and automation Systems based on PXI Express to have a data throughput of 6 GBytes/sec in each direction. PXI Express also offers two-way interoperability with CompactPCI Express products.

Instrumentation capabilities within PXI Express can reach a new level of performance by providing point-to-point differential triggers, point-to-point differential variable clocks, and a 100 MHz differential System clock. The highly used bussed triggers, point-to-point triggers, and 10 MHz clock defined in the PXI-1 specification are maintained. This allows PXI Express Module designers to make optimized cost versus performance tradeoffs when implementing instrumentation features.

PXI Express maintains compatibility with Modules designed to be compliant with the PXI-1 specification in two ways. First, PXI Express allows Chassis to have slots that are defined in the PXI-1 specification. Second, PXI Express defines a slot that accepts either a high-performance Module that uses PCI Express for data transfer or a Module designed to the PXI-1 specification that has had a connector change. Of course, this also means PXI Express allows for the compatibility with Modules designed to the CompactPCI specification.

By implementing PCI Express, PXI Express Systems can leverage the large base of existing industry-standard software. Desktop PC users have access to different levels of software, from operating systems to low-level device drivers to high-level instrument drivers to complete graphical APIs. All of these software levels can be used in PXI Express Systems. The PXI Systems Alliance maintains a separate Software Specification for PXI Express Modules, Chassis, and Systems. By having a separate Software Specification, the PXI Systems Alliance can more quickly adopt the latest operating Systems and software standards. PXI Express Modules, Chassis, and Systems developed to comply with this PXI Hardware Specification must also comply with the PXI-6: *PXI Express Software Specification*.

Figure 1-1 summarizes the scope of the *PXI Express Hardware Specification* by depicting its mechanical and electrical architectures.

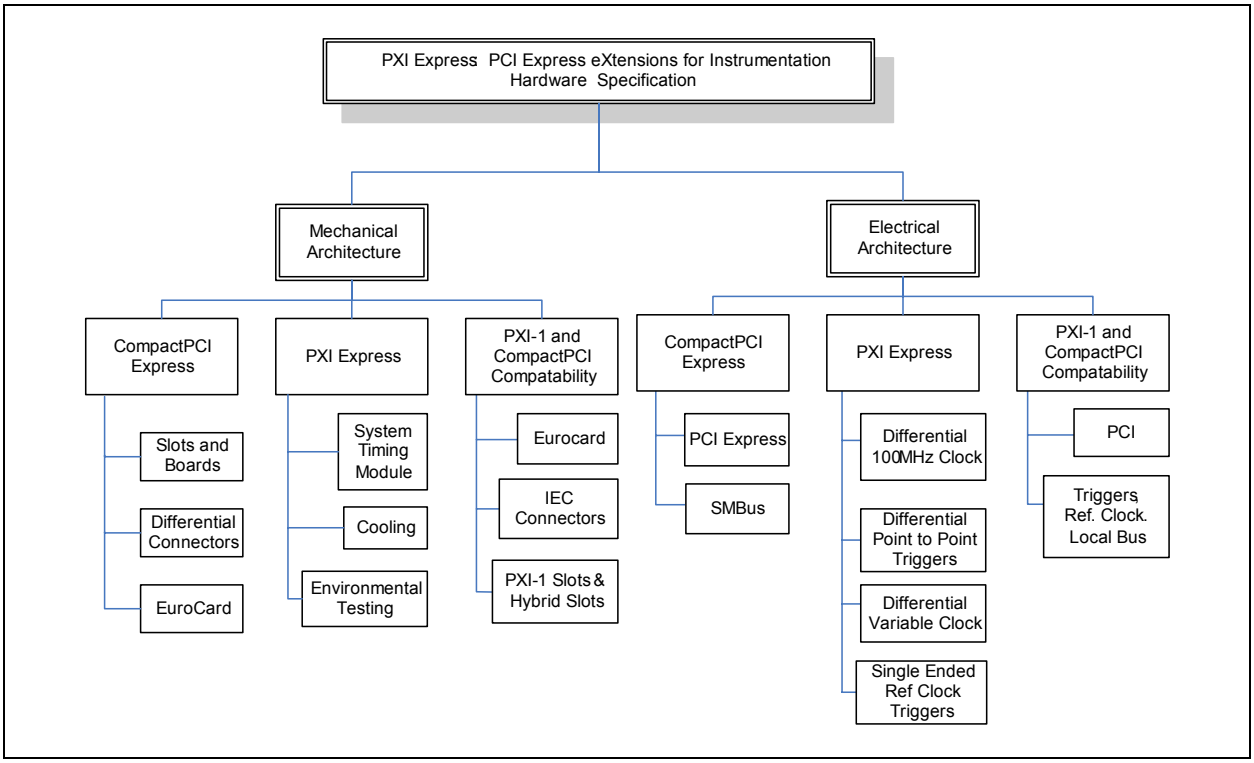

Figure 1-1. *PXI Express Hardware Specification* Architectures

Figure 1-2 summarizes the scope of the PXI-6: *PXI Express Software Specification* by depicting its architecture.

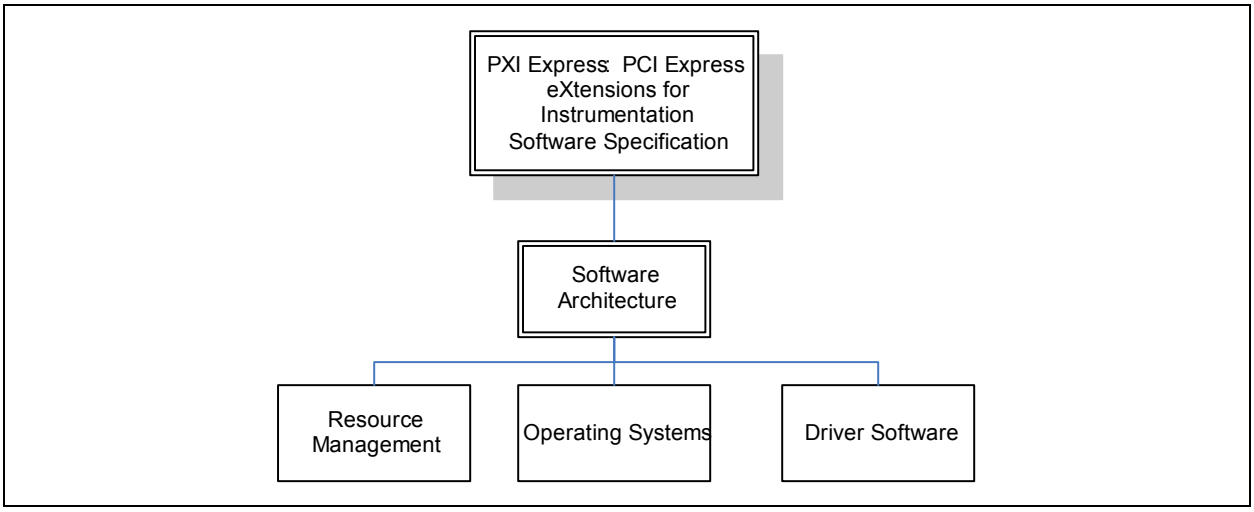

Figure 1-2. *PXI Express Software Specification* Architecture

1.2 Intended Audience and Scope

This specification is organized with a top-down approach whereby general descriptions precede the more detailed specifications found deeper in the subsections. This structure is intended to serve the needs of a variety of audiences from product developers to System integrators to end-users. Product developers may want to become familiar with all portions of this specification, while end users may be interested in only the feature set description and perhaps the summaries of how these features are implemented. The goal of this specification is to serve as the highest level document relevant to all users and providers of PXI Express compatible Systems, but in many cases this specification references other specifications such as CompactPCI Express and PXI-1 for certain details. These specifications and the specifications they in turn refer to may be needed to fully implement PXI Express products.

The first section of this specification describes the features that PXI Express Systems can offer and how these features can be applied to instrumentation. The subsequent sections cover the mechanical, electrical, and software requirements specific to implementing PXI Express features.

1.3 Background and Terminology

This section defines the acronyms and key words that are referred to throughout this specification. This specification uses the following acronyms:

- **API**—Application Programming Interface
- **CompactPCI**—PICMG 2.0 Specification
- **Eurocard**—European Packaging Specifications (IEC 60297, IEEE 1101.1, IEEE 1101.10, IEEE 1101.11)
- **GPIB**—General Purpose Interface Bus, IEEE 488
- **ISA**—Industry Standard Architecture; desktop PC adapter board specification
- **PCI**—Peripheral Component Interconnect; electrical specification defined by PCISIG
- **PCI Express**—Serialized evolution of PCI
- **PCI-SIG**—PCI Special Interest Group
- **PICMG**—PCI Industrial Computer Manufacturers Group
- **PXI**—PCI eXtensions for Instrumentation
- **PXI Express**—PCI Express eXtensions for Instrumentation
- **VISA**—Virtual Instrument Software Architecture
- **VITA**—VMEbus International Trade Association
- **VME**—Versa Module Europe; VMEbus specification governed by the VSO
- **VPP**—VXI*plug&play* Specification
- **VSO**—VITA Standards Organization
- **VXI**—VME Extensions for Instrumentation

This specification uses several key words, which are defined as follows:

RULE: Rules SHALL be followed to ensure compatibility. A rule is characterized by the use of the words SHALL and SHALL NOT.

RECOMMENDATION: Recommendations consist of advice to implementers that will affect the usability of the final Module. A recommendation is characterized by the use of the words SHOULD and SHOULD NOT.

PERMISSION: Permissions clarify the areas of the specification that are not specifically prohibited. Permissions reassure the reader that a certain approach is acceptable and will cause no problems. A permission is characterized by the use of the word MAY.

OBSERVATION: Observations spell out implications of rules and bring attention to things that might otherwise be overlooked. They also give the rationale behind certain rules, so that the reader understands why the rule must be followed.

MAY: A key word indicating flexibility of choice with no implied preference. This word is usually associated with a permission.

SHALL: A key word indicating a mandatory requirement. Designers SHALL implement such mandatory requirements to ensure interchangeability and to claim conformance with the specification. This word is usually associated with a rule.

SHOULD: A key word indicating flexibility of choice with a strongly preferred implementation. This word is usually associated with a recommendation.

1.4 Applicable Documents

This specification defines extensions to the base PCI Express and CompactPCI Express specifications referenced in this section. It is assumed that the reader has a thorough understanding of PCI Express and CompactPCI Express. The CompactPCI Express specification refers to several other applicable documents with which the reader may wish to become familiar. This specification refers to the following documents directly:

- PXI Software Specification (Latest Revision)
- PXI Hardware Specification (Latest Revision)
- *PCI Local Bus Specification*, Rev. 2.3
- *PCI Express Base Specification 1.1*
- *PCI Express Card Electromechanical (CEM) Specification 1.1*
- *PICMG 2.0 R3.0 CompactPCI Specification*
- *PICMG EXP.0 CompactPCI Express Specification*
- *System Management Bus (SMBus) Specification, Version 2.0*
- VXI*plug&play* Specifications (VPP-3.*x* and VPP-7)
- IEC 61326-1:1998, *Electrical equipment for measurement, control, and laboratory use—EMC requirements—Part I, General requirements*, International Electrotechnical Commission
- IEC 1010-1:1990 + A1:1992, *Safety requirements for electrical equipment for measurement, control, and laboratory use—Part 1, General requirements*, International Electrotechnical Commission
- IEC 60068-1, *Environmental testing*, International Electrotechnical Commission

1.5 Useful Web Sites

Below is a list of Web site links that at the time of publication of this specification point to sites with information useful in the understanding and design of PXI products:

- `http://www.pxisa.org/`—PXI specifications
- `http://www.picmg.org/`—PICMG specifications
- `http://www.ieee.org/`—IEEE specifications
- `http://www.iec.org/`—IEC specifications
- `http://www.pcisig.com/`—PCI and PCI Express specifications

- http://www.vita.com/—VME specifications
- http://www.vxi.org/—VXI specifications
- http://www.vxipnp.org/—VISA specifications
- http://www.smbus.org/—SMBus specification

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2. PXI Express Architecture Overview

This section presents an overview of PXI Express System features and capabilities by summarizing the mechanical, electrical, and software architectures defined by this specification.

2.1 Mechanical Architecture Overview

PXI Express supports 3U and 6U Module form factors just like PXI-1. Several new connectors have been added to support PCI-Express and are defined by the CompactPCI Express specification. This specification uses different names for the Module and slot types as compared to CompactPCI Express and introduces some new types as well. Table 2-1 shows the PXI Express component name and the equivalent CompactPCI Express component name.

Table 2-1. PXI Express and CompactPCI Express Specification Names

PXI Express Specification Name	CompactPCI Express Specification Name
PXI Express System Slot	System Slot
PXI Express System Module	System Board
PXI Express Peripheral Slot	Type 2 Peripheral Slot
PXI Express Peripheral Module	Type 2 Peripheral Board
PXI Express Hybrid Slot	Hybrid Slot
Hybrid Slot Compatible PXI-1 Module	N/A
PXI Express System Timing Slot	N/A
PXI Express System Timing Module	N/A
PXI-1 Slot	Legacy Slot
PXI-1 Module	CompactPCI Peripheral Board

The Module and slot types used from the CompactPCI Express specification as well as the new ones introduced by this specification are described in the following sections.

2.1.1 Module and Slot Types

PXI Express Module and slot types include a 3U and 6U PXI Express System Module and Slot, a 3U and 6U PXI Express Peripheral Module and Slot, a PXI Express 3U and 6U Hybrid Peripheral Slot, a 3U and 6U PXI Express System Timing Module and Slot, a 3U and 6U Hybrid Slot, and a 3U and 6U Hybrid Slot compatible PXI-1 Module. In addition to these Module and slot types, 3U and 6U PXI Peripheral Slots defined in the PXI-1 specification are allowed in PXI Express Chassis to support PXI-1 Peripheral Modules.

2.1.1.1 3U and 6U PXI Express System Module and Slot

PXI Express System Modules have four required connectors, XP1/XJ2/XJ3/XJ4, as defined by the CompactPCI Express specification. A simplified description of the connector functionality is XP1/XJ1 is for power, XP2/XJ2 and XP3/XJ3 are for PCI Express, and XP4/XJ4 is for instrumentation signals defined in the PXI-1 specification. The 6U System Module may use J3/J4/J5 for rear I/O applications.

Figures 2-1 and 2-2 show the 3U and 6U PXI Express System Modules, respectively.

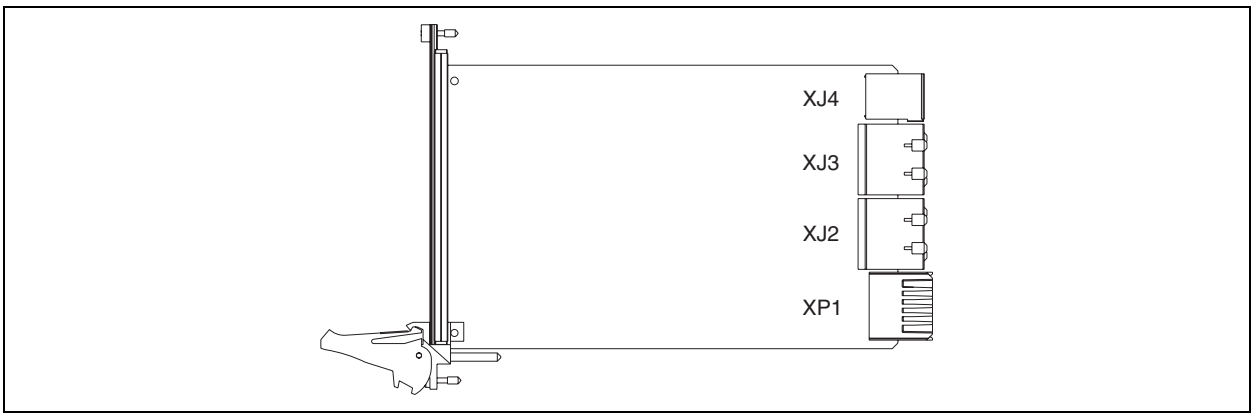

Figure 2-1. 3U PXI Express System Module

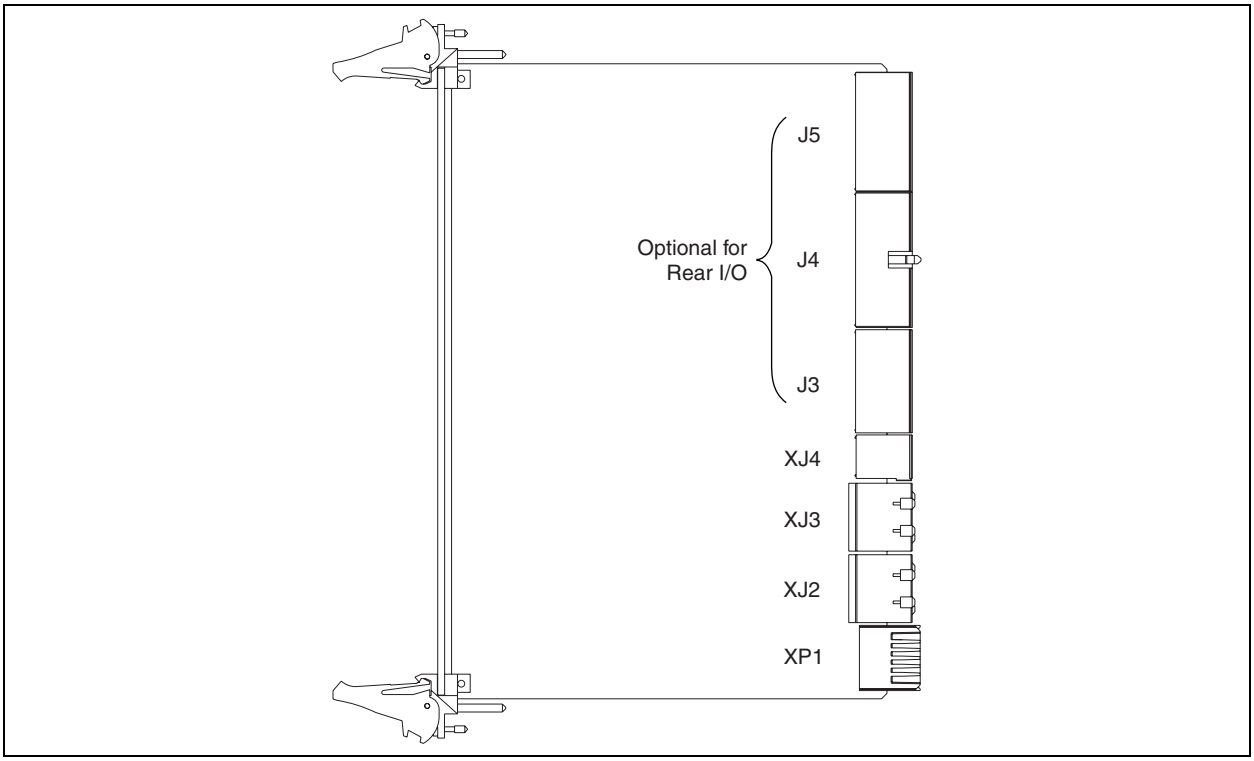

Figure 2-2. 6U PXI Express System Module

Figures 2-3 and 2-4 show the 3U and 6U PXI Express System Slots, respectively.

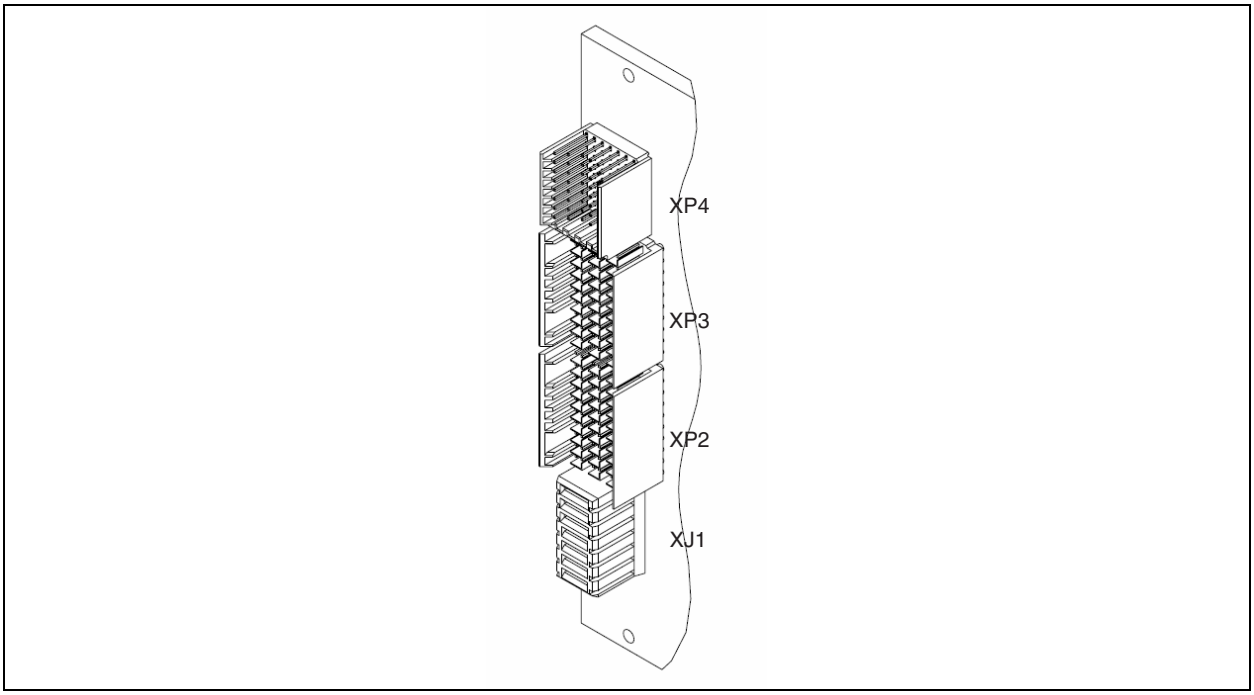

Figure 2-3. 3U PXI Express System Slot

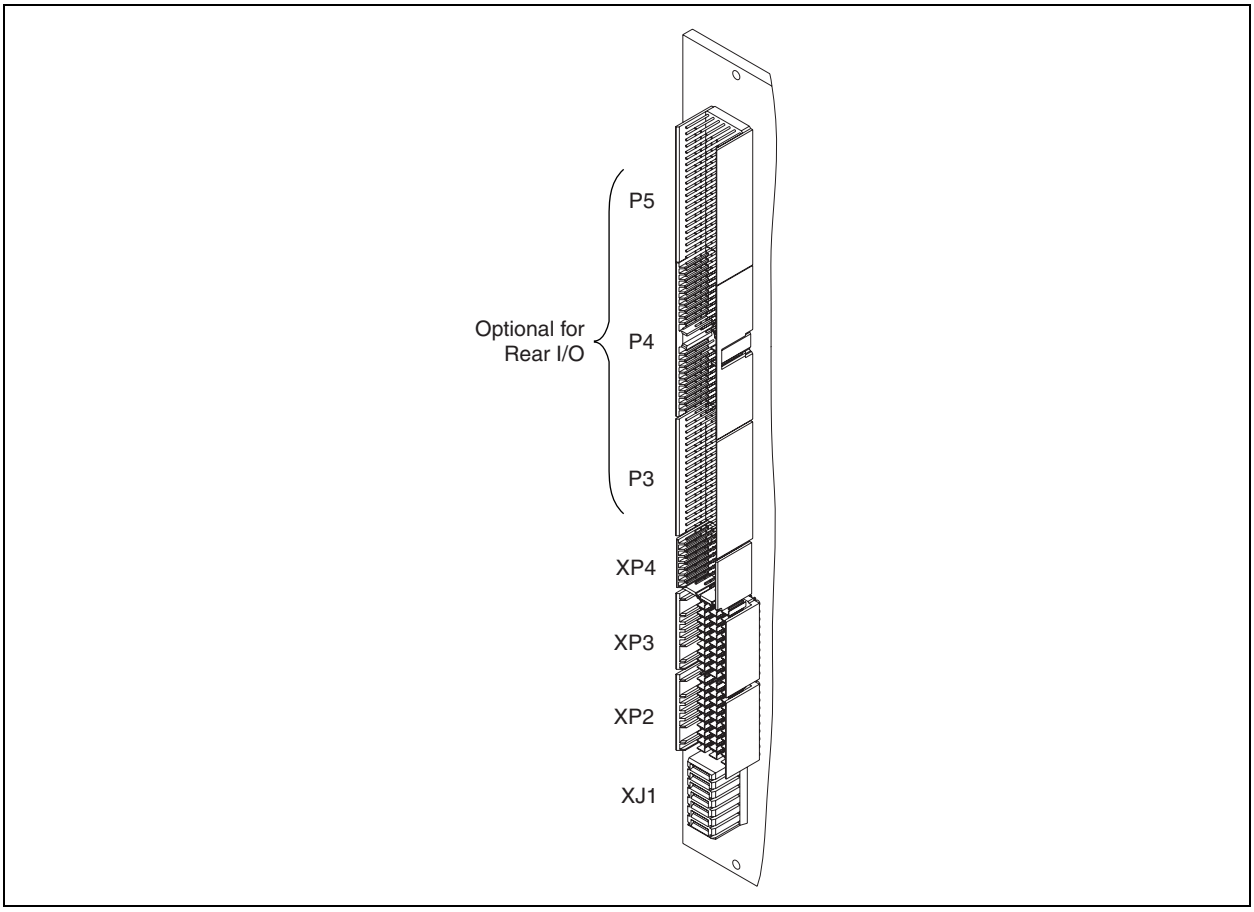

Figure 2-4. 6U PXI Express System Slot

2.1.1.2 3U and 6U PXI Express Peripheral Module and Slot

The 3U PXI Express Peripheral Module has two connectors, XJ3 and XJ4. A simplified description of the connector functionality is that XP3/XJ3 are for PCI Express and Differential Triggers and Timing, and XP4/XJ4 is for instrumentation signals that are defined in the PXI-1 specification. The 6U PXI Express Peripheral Module has an Optional eHM connector (required for backplanes), XJ8, that is populated in the upper columns of the legacy J5 location to provide additional power to the 6U Module. The PXI Express specification does not support the use of J3/J4/J5 on 6U Peripheral Modules.

Figures 2-5 and 2-6 show the 3U and 6U PXI Express Peripheral Modules, respectively.

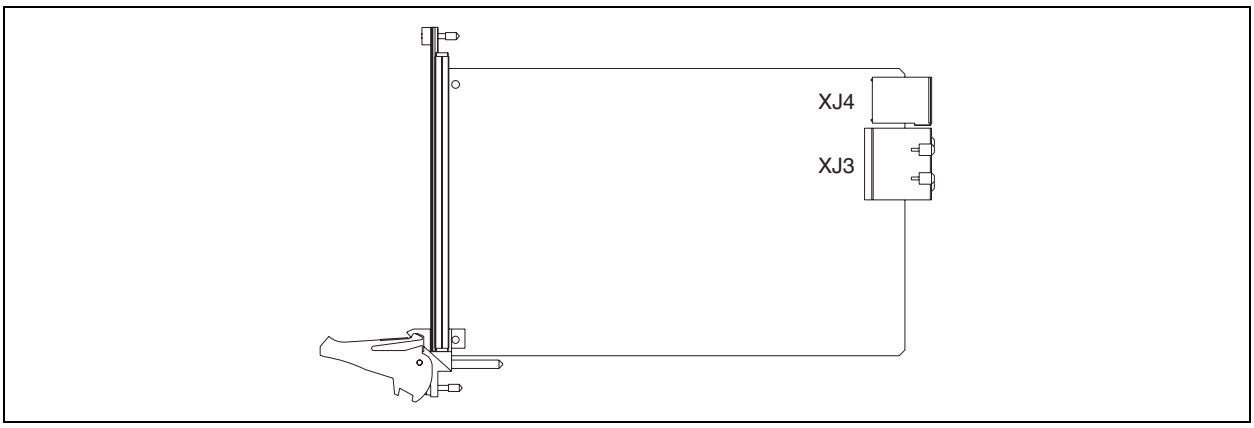

Figure 2-5. 3U PXI Express Peripheral Module

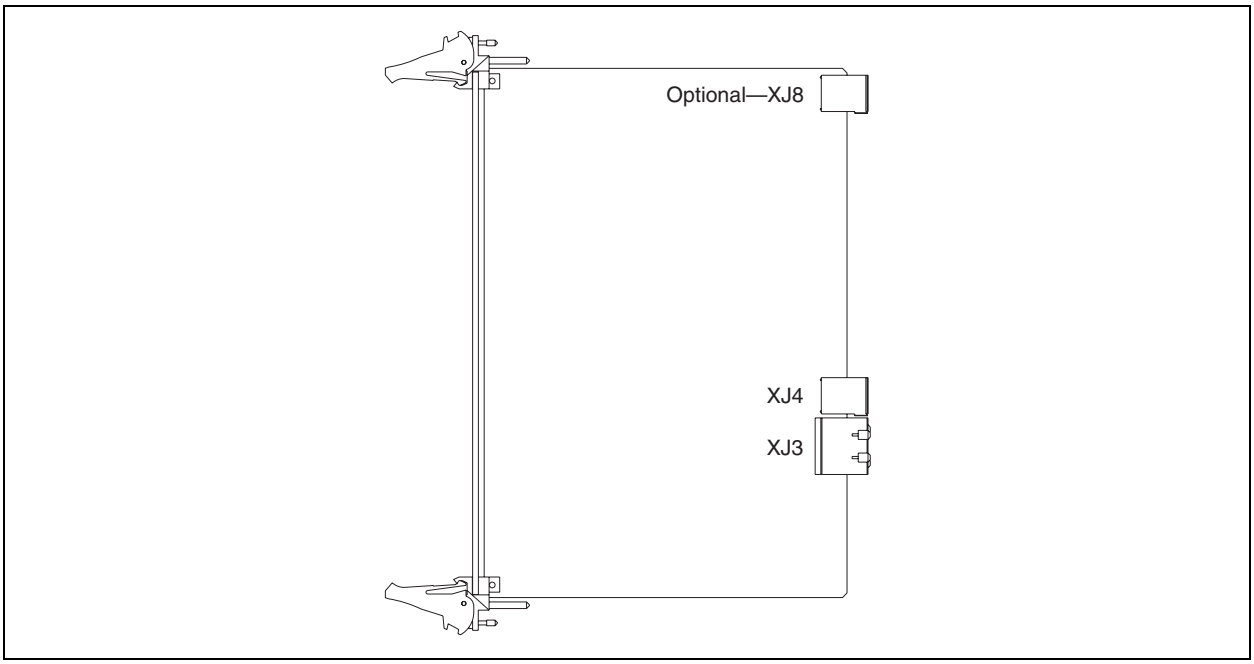

Figure 2-6. 6U PXI Express Peripheral Module

Figures 2-7 and 2-8 show the 3U and 6U PXI Express Peripheral Slots, respectively.

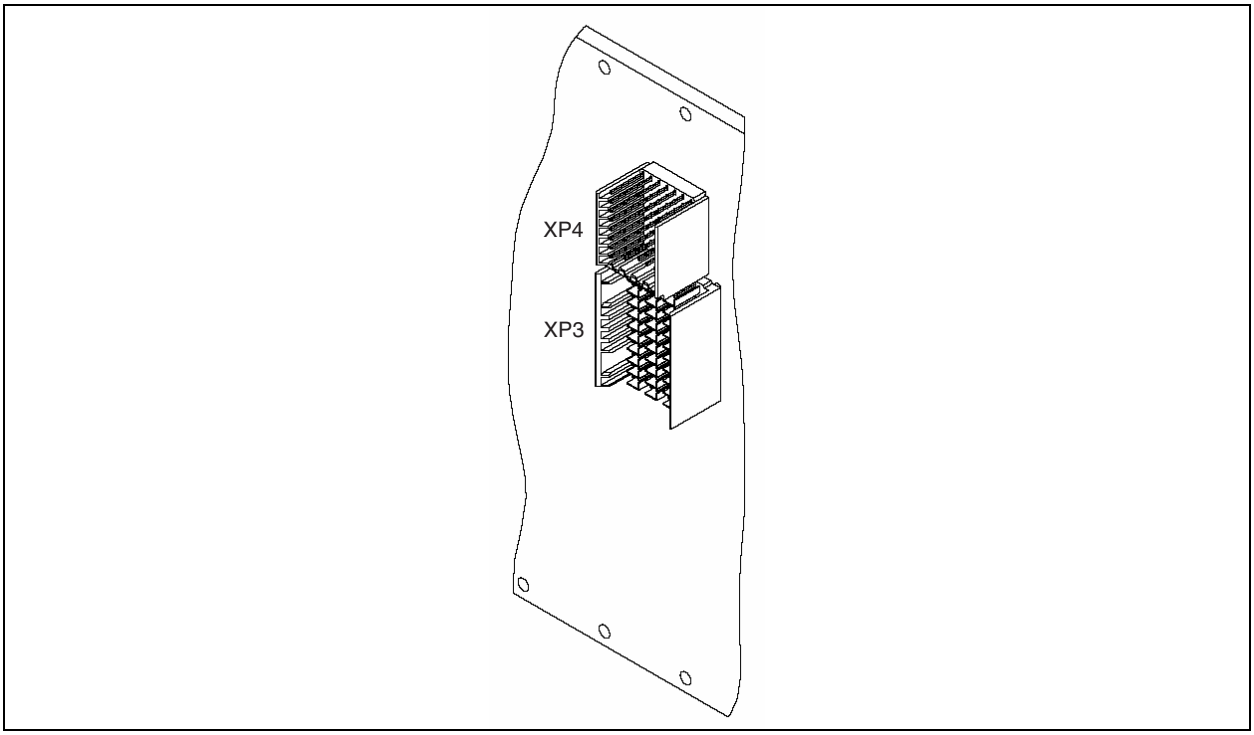

Figure 2-7. 3U PXI Express Peripheral Slot

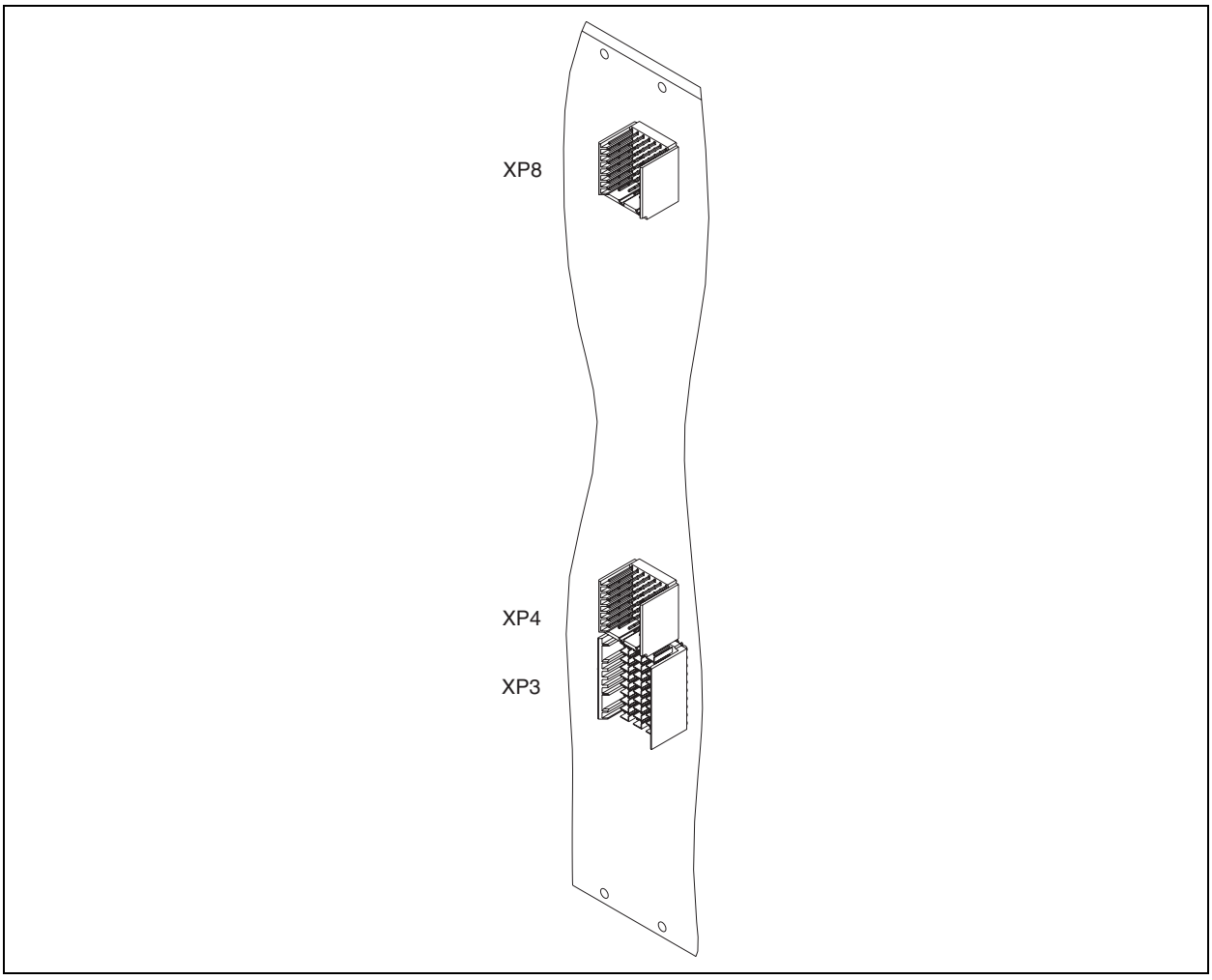

Figure 2-8. 6U PXI Express Peripheral Slot

2.1.1.3 3U and 6U PXI Express Hybrid Peripheral Slot

3U Hybrid Peripheral Slots have three connectors: P1, XP3, and XP4. A simplified description of the connector functionality is that P1/J1 are for 32 bit PCI, XP3/XJ3 are for PCI Express and Differential Triggers and Timing, and XP4/XJ4 is for instrumentation signals defined in the PXI-1 specification. 6U Hybrid Peripheral Slots have four connectors: P1, XP3, XP4, and XP8. P3, P4, and P5 are not allowed.

Figures 2-9and 2-10 show the 3U and 6U PXI Express Hybrid Slots, respectively.

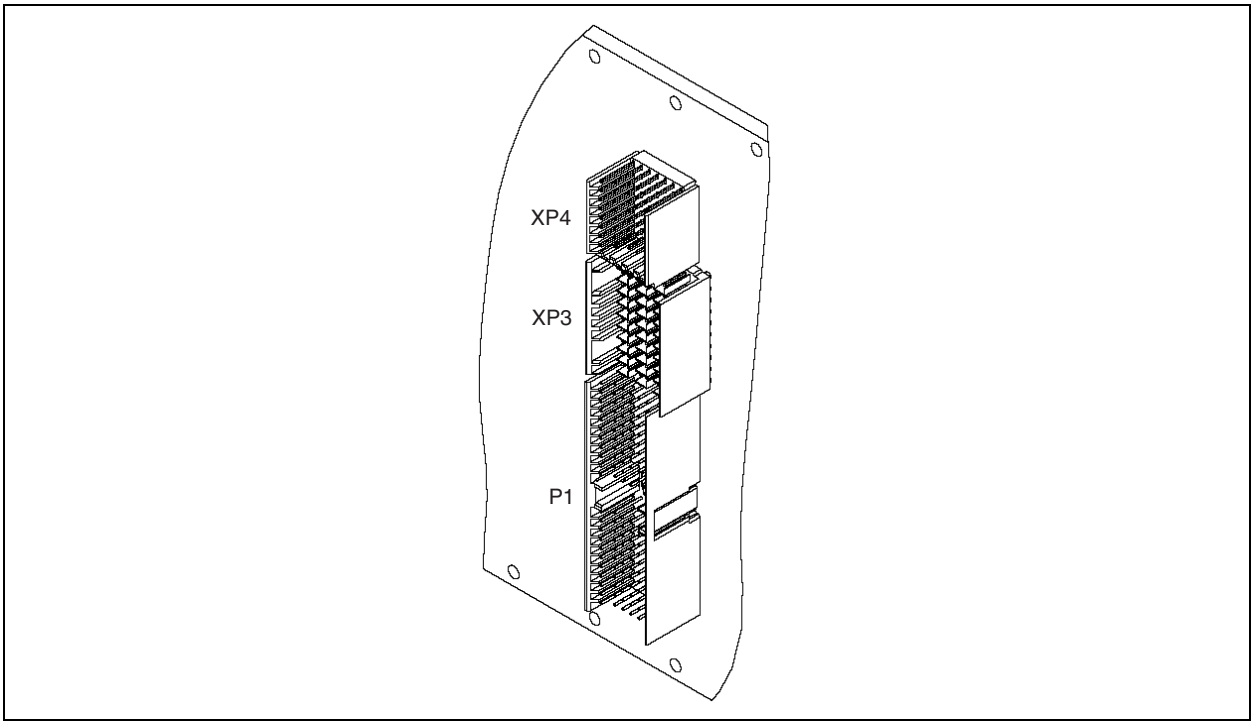

Figure 2-9. 3U PXI Express Hybrid Peripheral Slot

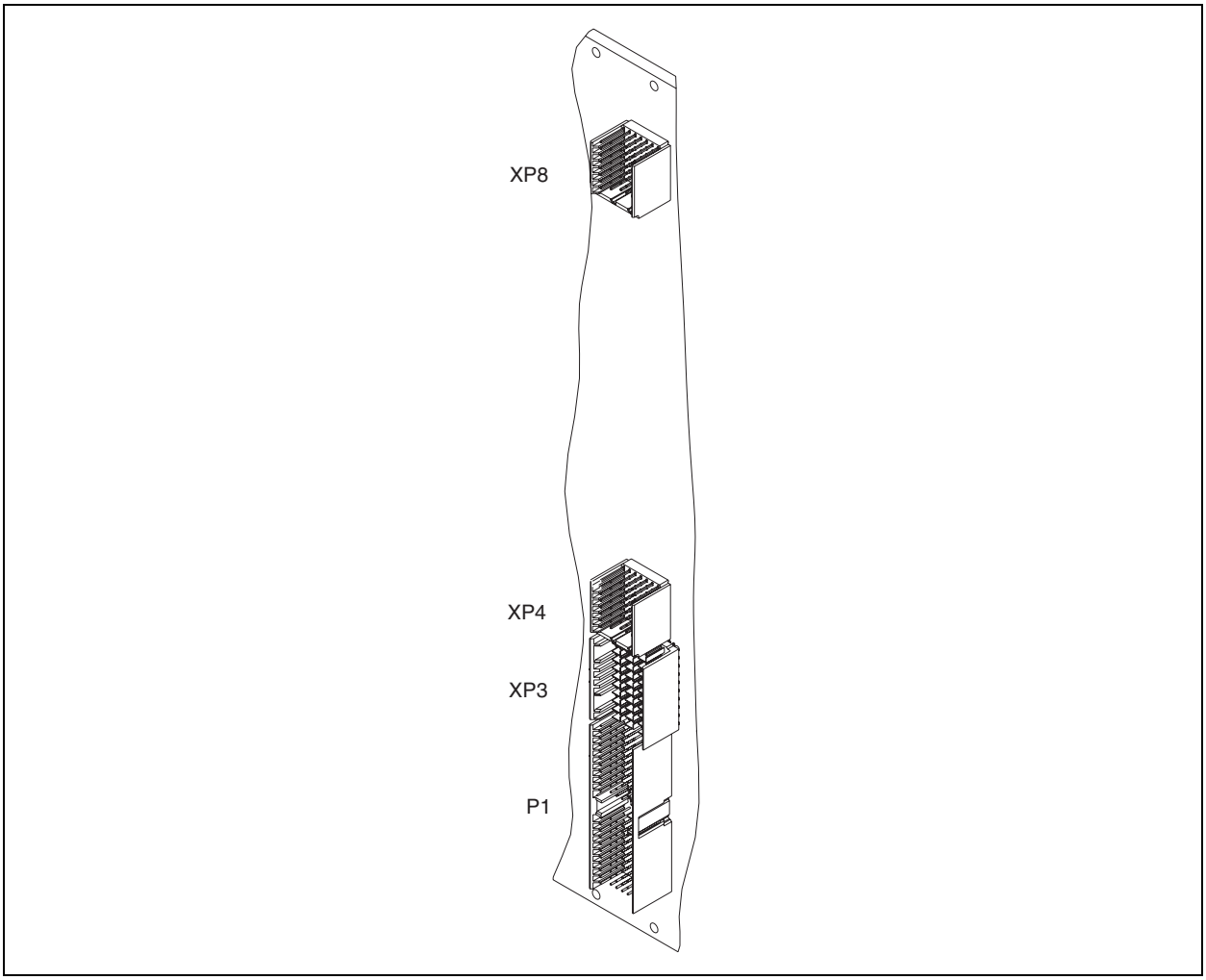

Figure 2-10. 6U PXI Express Hybrid Peripheral Slot

2.1.1.4 3U and 6U PXI Express System Timing Module and Slot

PXI Express introduces new 3U and 6U Modules called a System Timing Module. It also introduces the associated slots for 3U and 6U called a System Timing Slot.

The 3U System Timing Module has four connectors, TJ1, TJ2, XJ3 and XJ4, as shown in Figure 2-11. A simplified description of the connector functionality is TJ1/TP1 and TJ2/TP2 are for fanout of the Differential and Star Triggers, XP3/XJ3 are for PCI Express and Differential Triggers and Timing, and XP4/XJ4 is for instrumentation signals that are defined in the PXI-1 specification.

The 3U Slot has three required connectors: TP2, XP3, and XP4. TP1 is Optional for backplanes that have seven or fewer slots requiring differential triggers.

A 6U System Timing Module has the same connectors as the 3U Timing Module, plus the Optional XJ8 connector for additional power.

A 6U System Timing Module designed for 6U Chassis that support stacking 3U Modules with more than 18 Slots has the additional TJ5 and TJ6 connectors. This allows the 6U System Timing Module to connect to additional triggers.

A 6U System Timing Slot that does not allow stacking 3U System Timing Modules has four required connectors: TP2, XP3, XP4, and XP8. TP1 is Optional for backplanes with seven or fewer slots requiring differential triggers.

A 6U System Timing Slot that supports stacking 3U System Timing Modules has seven required connectors: TP1, TP2, XP3, XP4, upper TP2, upper XP3, and upper XP4. The upper TP1 connector is Optional for backplanes with 24 or fewer slots requiring differential triggers.

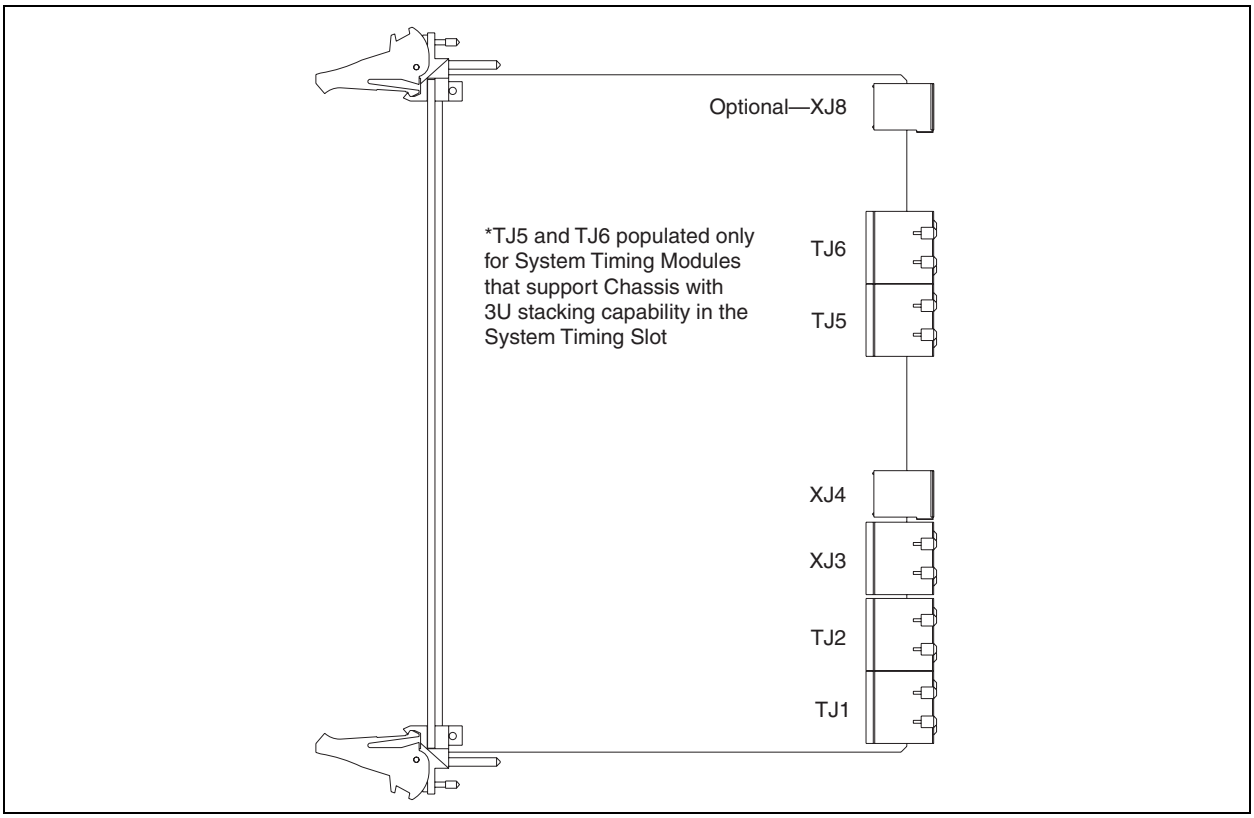

Figure 2-11. 6U PXI Express System Timing Module

The 3U PXI Express System Timing Slot is shown in Figure 2-12.

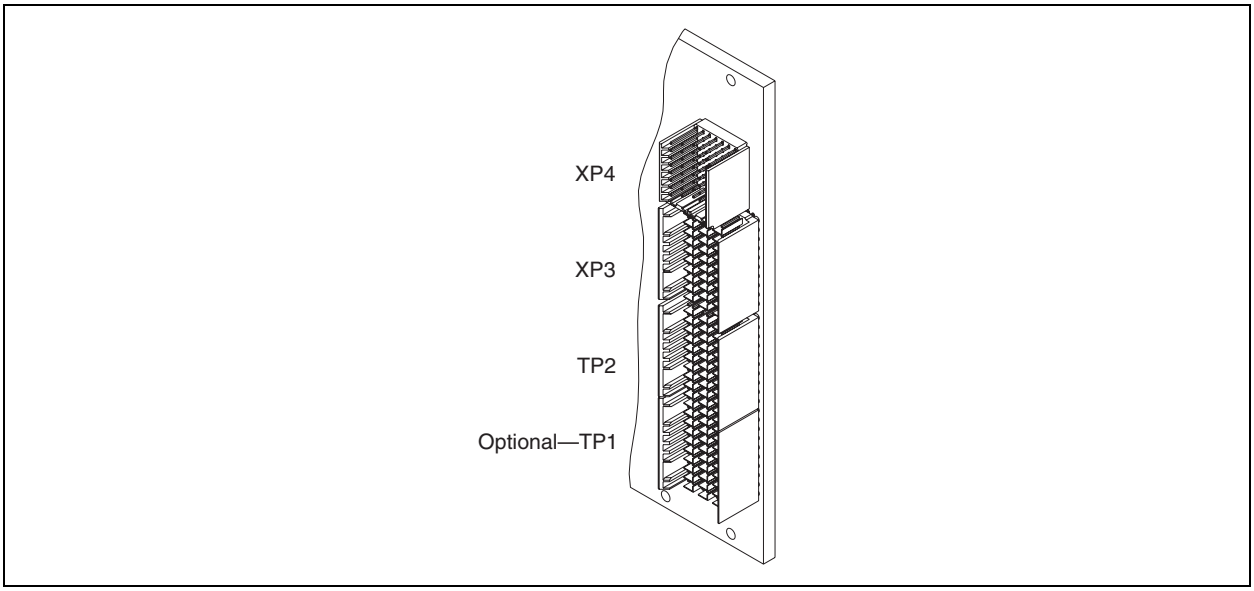

Figure 2-12. 3U PXI Express System Timing Slot

The 6U Timing Module Slot is shown in Figures 2-13 and 2-14.

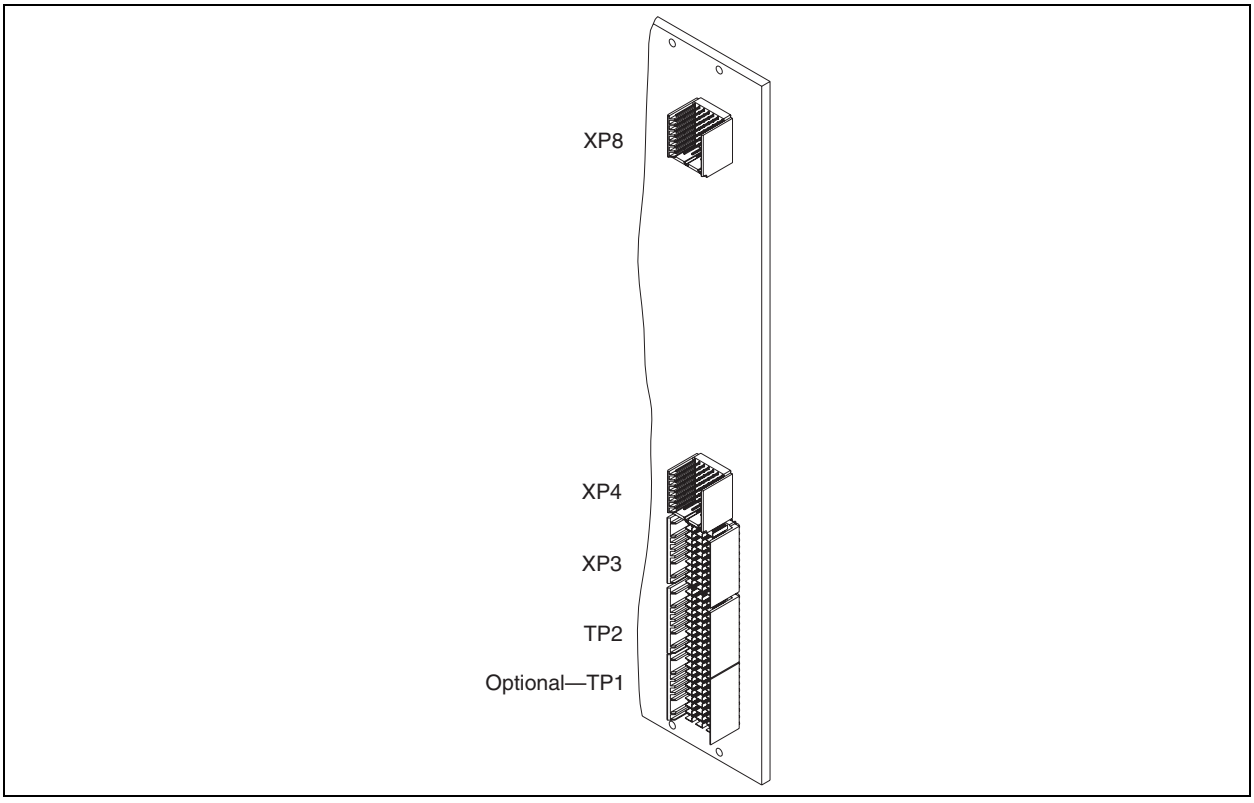

Figure 2-13. 6U PXI Express System Timing Slot

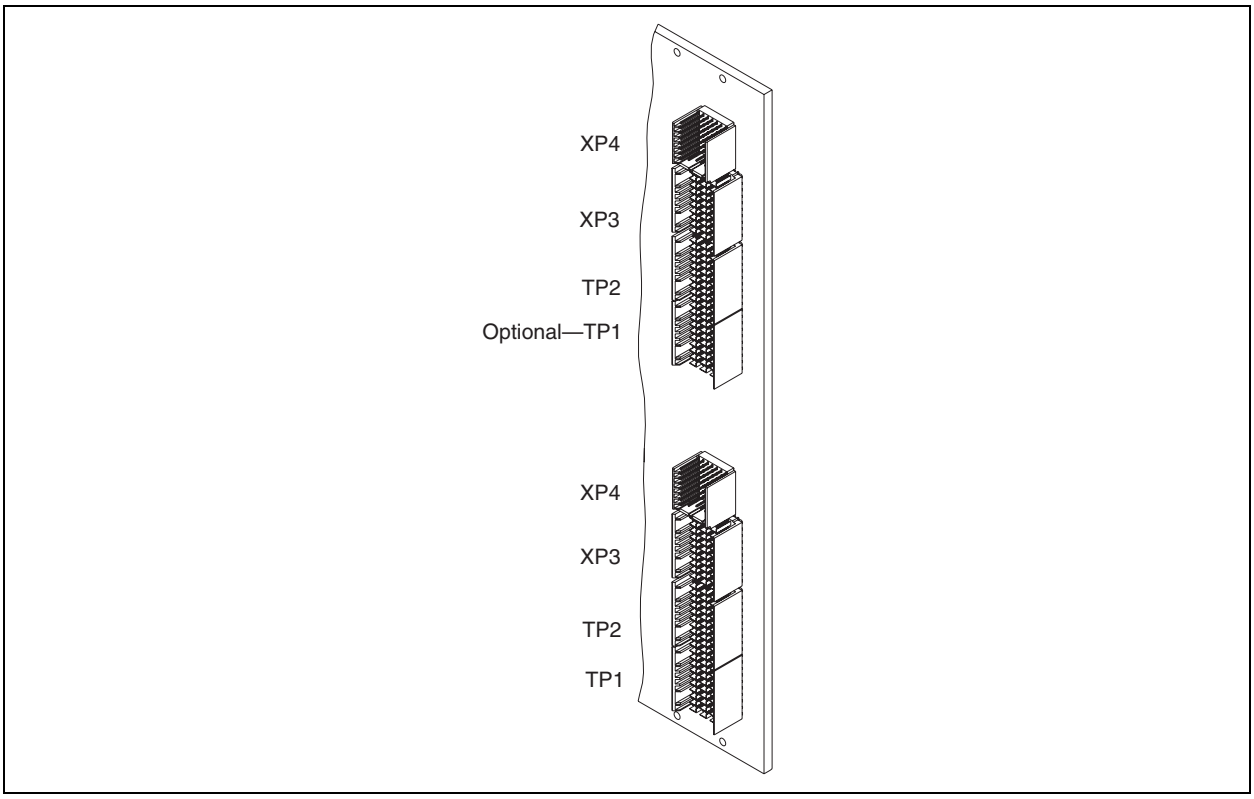

Figure 2-14. 6U PXI Express System Timing Slot with Stacked 3U Support

2.1.1.5 PXI-1 Slot

In a PXI Express Chassis, there may be slots that support PXI boards as they are defined in PXI-1 (*PXI Hardware Specification*, Revision 2.2). These slots meet the mechanical requirements of the *PXI Hardware Specification* and are referred to as PXI-1 slots.

2.1.1.6 3U and 6U Hybrid Slot Compatible PXI-1 Peripheral Module

PXI-1 or an associated ECN defines a 3U and 6U Hybrid Slot Compatible PXI-1 Peripheral Module that consists of a 3U or 6U PXI-1 Module where the J2 HM connector has been replaced with an eHM connector. The eHM connector is a modified 2 mm HM connector that includes application keying and is installed in the same location as the upper eight columns of the PXI-1 J2 connector. This board type may be used in any PXI-1 or PXI Express Hybrid Slot. Figures 2-15 and 2-16 show the 3U and 6U Hybrid Slot Compatible PXI-1 Modules.

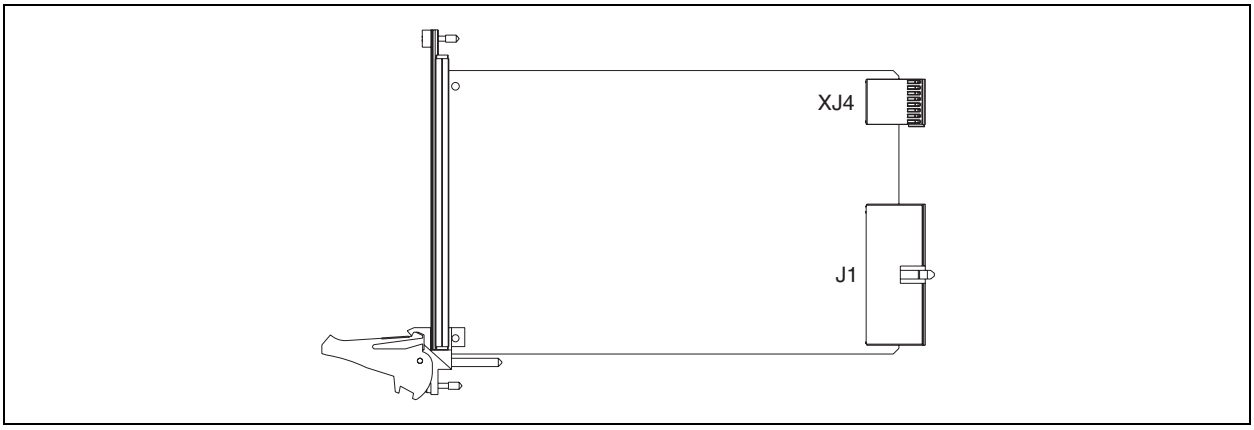

Figure 2-15. 3U Hybrid Peripheral Slot Compatible PXI-1 Module

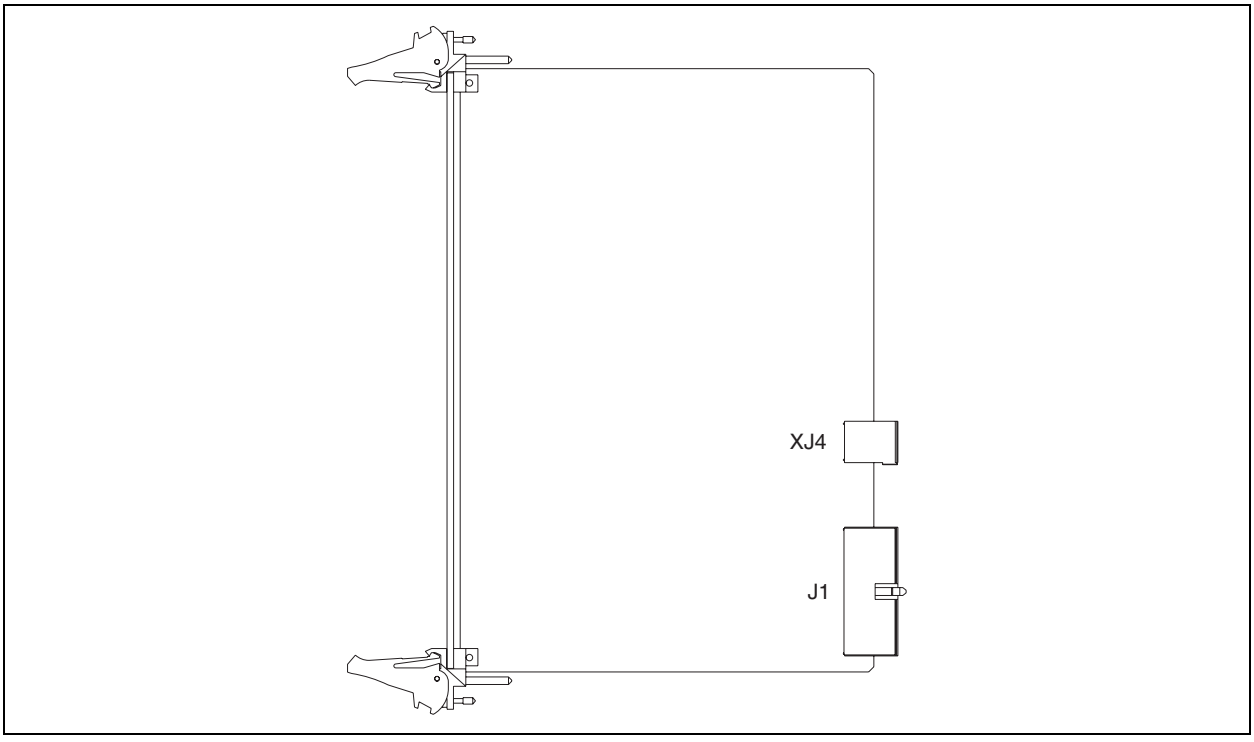

Figure 2-16. 6U Hybrid Peripheral Slot Compatible PXI-1 Module

2.1.2 System Slot and System Timing Module Location

PXI Express defines the System Slot location to be the furthest left slot within a Chassis and to be numbered Slot 1. This defined arrangement is a subset of the numerous possible configurations allowed by CompactPCI Express (a CompactPCI Express System Slot may be located anywhere on a backplane). Defining a single location for the System Slot simplifies integration and increases the degree of compatibility between PXI Express Controllers and Chassis. Furthermore, the *PXI Express Hardware Specification* requires that, if necessary, the System Module should expand to the left into what are defined as Controller expansion slots. Expanding to the left prevents System Modules from using up valuable Peripheral Slots.

Some PXI Express Chassis may integrate the System Module functionality within the Chassis. In such a system, a System Slot is not required, and Peripheral Slots begin their numbering with 2.

PXI Express defines a System Timing Slot that can accept a PXI Express Peripheral Module or a System Timing Module that can provide individual triggers to all other Peripheral Modules and allow the replacement of the System reference clock. The location of the System Timing Slot is not mandated by the specification, which allows backplane designers to optimize the backplane for cost.

2.1.3 Additional Mechanical Features

In addition to the features defined by the PXI-1 Specification, PXI Express has added additional suggestions for cooling and for the measurement and specification of acoustic noise levels.

2.1.4 Interoperability with CompactPCI Express

Interoperability among PXI Express-compliant products and standard CompactPCI Express products is a very important feature provided by this specification and the CompactPCI Specification. Some PXI Express-compatible systems may require components that do not implement PXI Express-specific features. For example, a user may want to use a standard CompactPCI Express network interface Module in a PXI Express Chassis. Likewise, some users may choose to use a PXI Express-compatible Module in a standard CompactPCI Express Chassis. In these cases, the user cannot use PXI Express-specific Functions, but still can use the basic Module Functions.

Note that interoperability between PXI Express products and other application-specific implementations of CompactPCI Express products (which may define other signal definitions for the I/O pins of the XP4/XJ4 connectors) is not guaranteed. The CompactPCI Express specification provides mechanical keying of the XP4/XJ4 connectors for both PXI Express products and application-specific CompactPCI Express products to prevent electrical conflict between them.

2.1.5 Typical System Components

Figure 2-17 presents an example PXI Express system to help illustrate the following key words (in *italics*). A PXI Express System is composed of a *Chassis* that supports the PXI Express *backplane* and provides the means for supporting the System Controller and Peripheral *Modules*. The Chassis may have one *System Slot* and must have one or more *Peripheral Slots*. Any number of *System Expansion Slots* may be available to the left of the System Slot. The *System Timing Slot* may reside in any of the available slots to the right of Slot 1. The backplane carries the *interface connectors* (XP1,XJ2, etc.) and provides the interconnection between the Controller, Peripheral and Timing Slots.

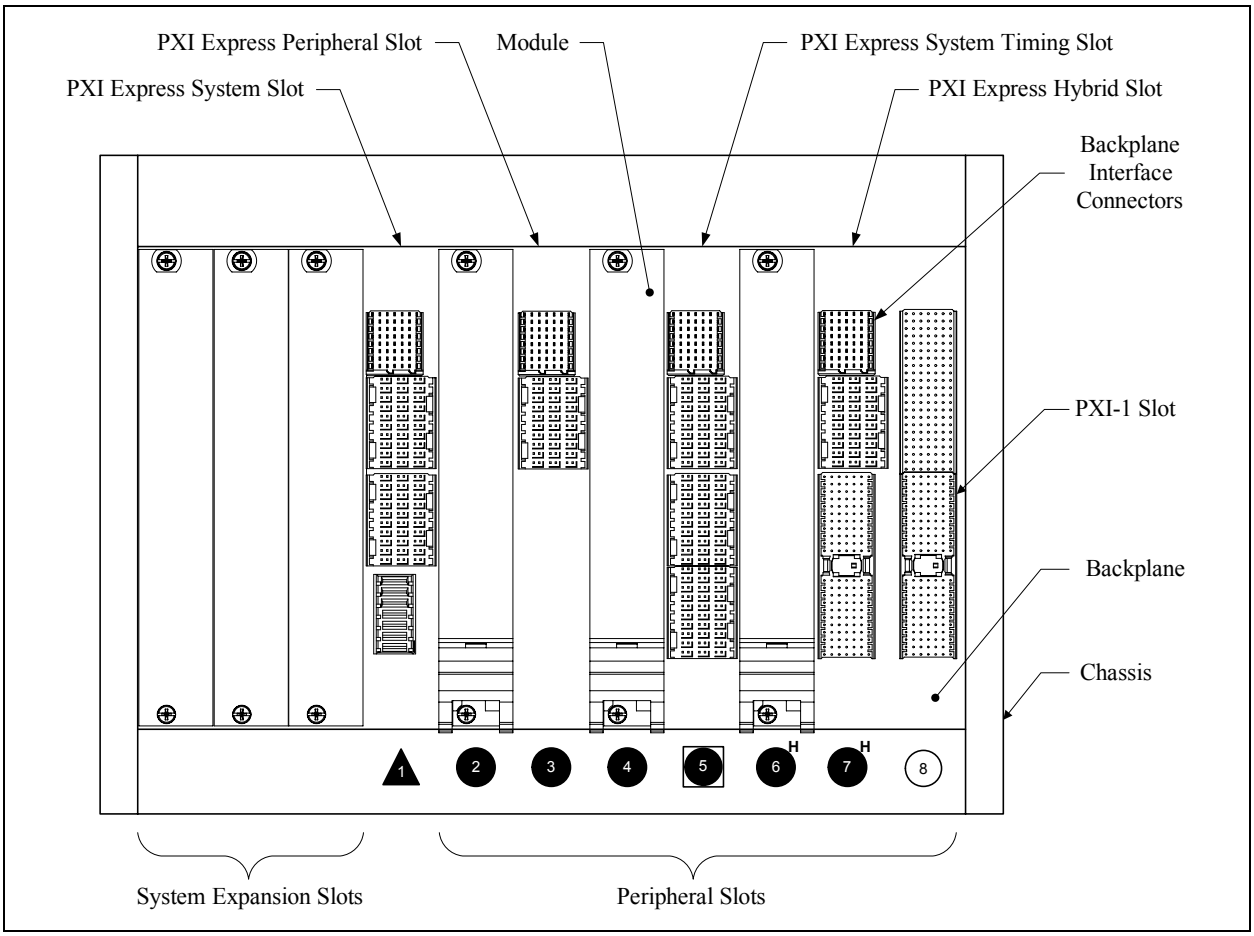

Figure 2-17. Typical System Components

2.1.6 Chassis Supporting Stacking 3U Modules in a 6U Slot

Just as with the PXI-1 Specification, PXI Express allows for efficient use of 3U Modules in a 6U Chassis. 6U PXI Express Chassis can support stacking of certain combinations of 3U Modules in a single 6U Slot. This allows one 3U Module to be plugged into the lower position of a 6U Slot, and another 3U Module to be plugged into the upper position of the same 6U Slot simultaneously. This can be accomplished mechanically using a 3U/3U adapter or using commercially available Subrack center extrusions. A 6U PXI Express Chassis may have any number of 6U Slots that support this feature. Figure 2-18 shows a general configuration of a 6U Chassis supporting 3U Module stacking. A 6U PXI Express Chassis may have any number of 6U Slots that support this feature.

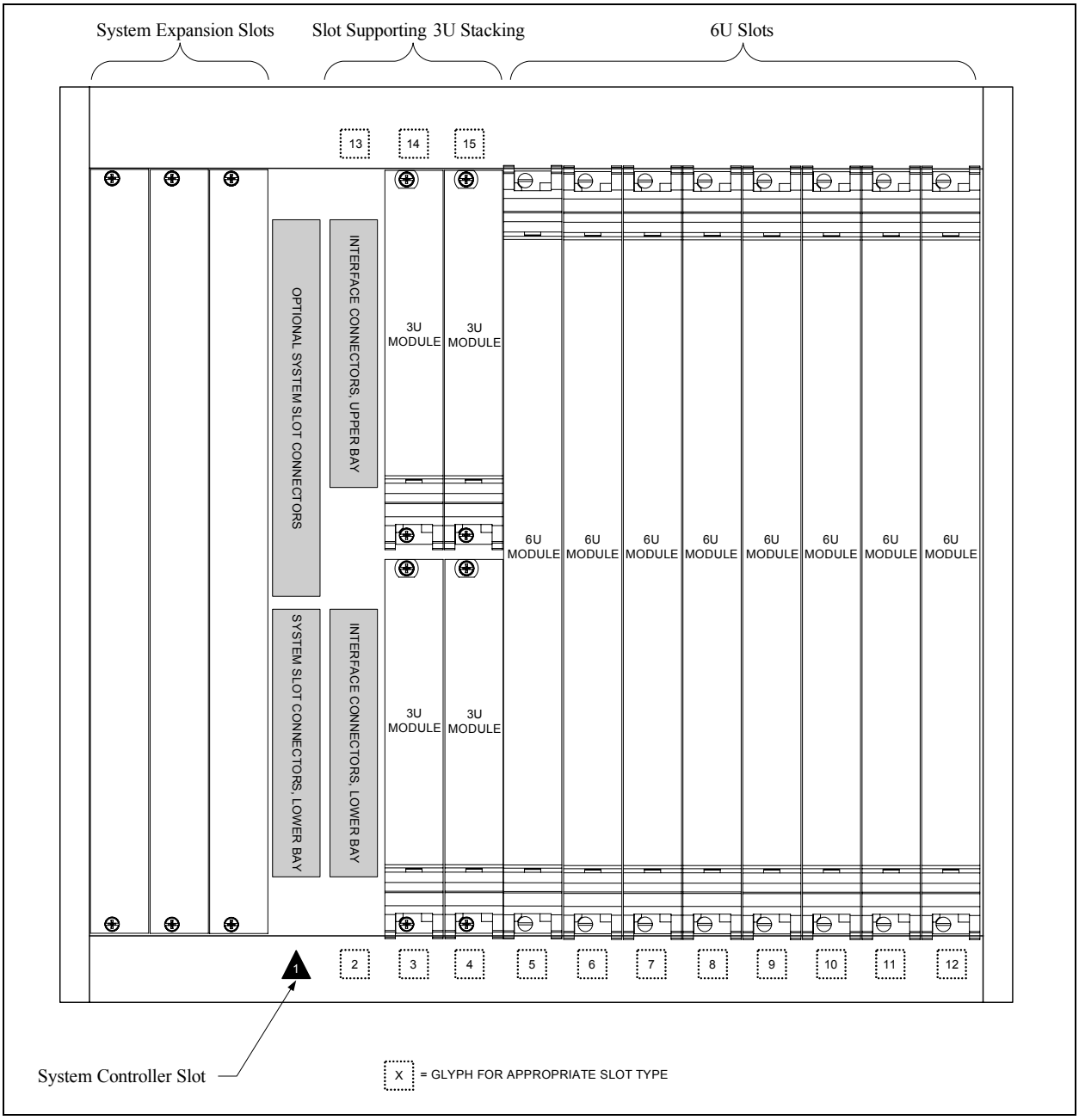

Figure 2-18. Example of a PXI Express Chassis that Supports 3U Stacking

2.2 Electrical Architecture Overview

In the same way that PXI combined instrumentation features with the desktop computer bus standard of PCI, PXI Express combines instrumentation features with the new desktop computer bus standard of PCI Express. The instrumentation features of PXI Express include many of the PXI instrumentation features, as well as a new differential 100 MHz system clock, new point-to-point differential triggers, and a new point-to-point variable frequency clock. These features are implemented on the backplane for the highest performance instrumentation timing and synchronization.

2.2.1 Features Leveraged from CompactPCI Express

PCI Express is one of the main features that PXI Express leverages from CompactPCI Express. PXI Express Systems can have up to 6 GBytes/sec per direction of data moving to and from the System Module, and an individual PXI Express Peripheral Module can have up to 2 GB per direction. Considering that PCI Express Switches have the ability for multiple separate data paths to be transferring data between PCI Express devices at the same time, the possibility exists for data rates above 32 GB/s per direction within a PXI Express System. The amount of bandwidth for a system is implementation specific and allows PXI Express suppliers to develop systems that meet their customers' needs in terms of cost and performance.

Electrical rules that are leveraged from the CompactPCI Express specification into PXI Express include but are not limited to the following:

- PCI Express transmit and receive electrical signaling definitions and budgets
- PCI Express reference clock
- PCI Express sideband signals
- SMBus
- Backplane identification and capability via SMBus
- Signals used for power supply control
- Power supply requirements
- Module and slot pin assignments with the exception of the additional instrumentation signals
- PCI with certain slot types

Table 2-2 shows the components that are interoperable between the two specifications. Note that when PXI Express Modules are used in CompactPCI Express Chassis, the PXI Express Module's instrumentation features are not usable.

Table 2-2. PXI and PXI Express Module Interoperability

PXI Express Component	CompactPCI Express Component						
	System Slot	**System Board**	**Type 2 Peripheral Slot**	**Type 2 Peripheral Board**	**Hybrid Slot**	**Legacy Slot**	**CompactPCI Peripheral Board**
PXI Express System Slot		OK					
PXI Express System Module	OK						
PXI Express Peripheral Slot				OK			
PXI Express Peripheral Module			OK		OK		
PXI Express Hybrid Slot				OK			OK [1]
Hybrid Slot Compatible PXI-1 Module					OK	OK	
System Timing Slot				OK			
System Timing Module			OK				
PXI-1 Slot							OK
PXI-1 Module						OK	

[1] CompactPCI Peripheral Board will work if it has J1 only.

2.2.2 Features Leveraged from the PXI Hardware Specification

PXI Express products can take advantage of the increase in data performance while implementing the instrumentation features in the PXI-1 Specification. Each PXI Express Module and slot type defined in this specification can leverage the PXI 10 MHz system clock (PXI_CLK10), the PXI-bused trigger lines, a Local Bus line, and PXI star trigger as defined in the PXI-1 Specification, in addition to the new instrumentation features defined in this specification. PXI-1 slots implemented in PXI Express systems also maintain the PXI Local Bus. PXI Express slots have the potential for a virtual local bus by taking advantage of PCI Express Switches allowing multiple data paths to transfer data between PCI Express devices at the same time. Determinism of data movement with such a virtual local bus may be PCI Express Switch and data dependent.

2.2.3 New Instrumentation Features

The system timing and synchronization capabilities of PXI are a key differentiation from other instrumentation form factors. PXI was created by adding those features to the high-bandwidth PCI bus and compact modular form factor of CompactPCI while maintaining reasonable implementation cost. The timing and triggering capabilities of PXI are retained in this specification and will continue to solve many system applications in PXI. With the advances in technology affording higher performance, low-cost differential signaling, and the differential connectors necessary for PCI Express already required, PXI Express builds on the existing capabilities by providing a differential system clock, differential synchronization, and differential star trigger and clock signals from a new System Timing Module. The key advantages of providing differential clocking and synchronization is the increased noise immunity provided to instrumentation clocks and the ability to transmit higher frequency clocks. These high-frequency clocks not only allow for higher performance, but also match well with modern processes and allow for low-cost products to remove clock multiplication circuits in many cases. The new features are added in a way to be compatible and highly interoperable with existing PXI Modules. The following sections will describe the new additions. Figure 2-19 shows one example of how the instrumentation signals are implemented on a PXI Express backplane that has a System Timing Slot.

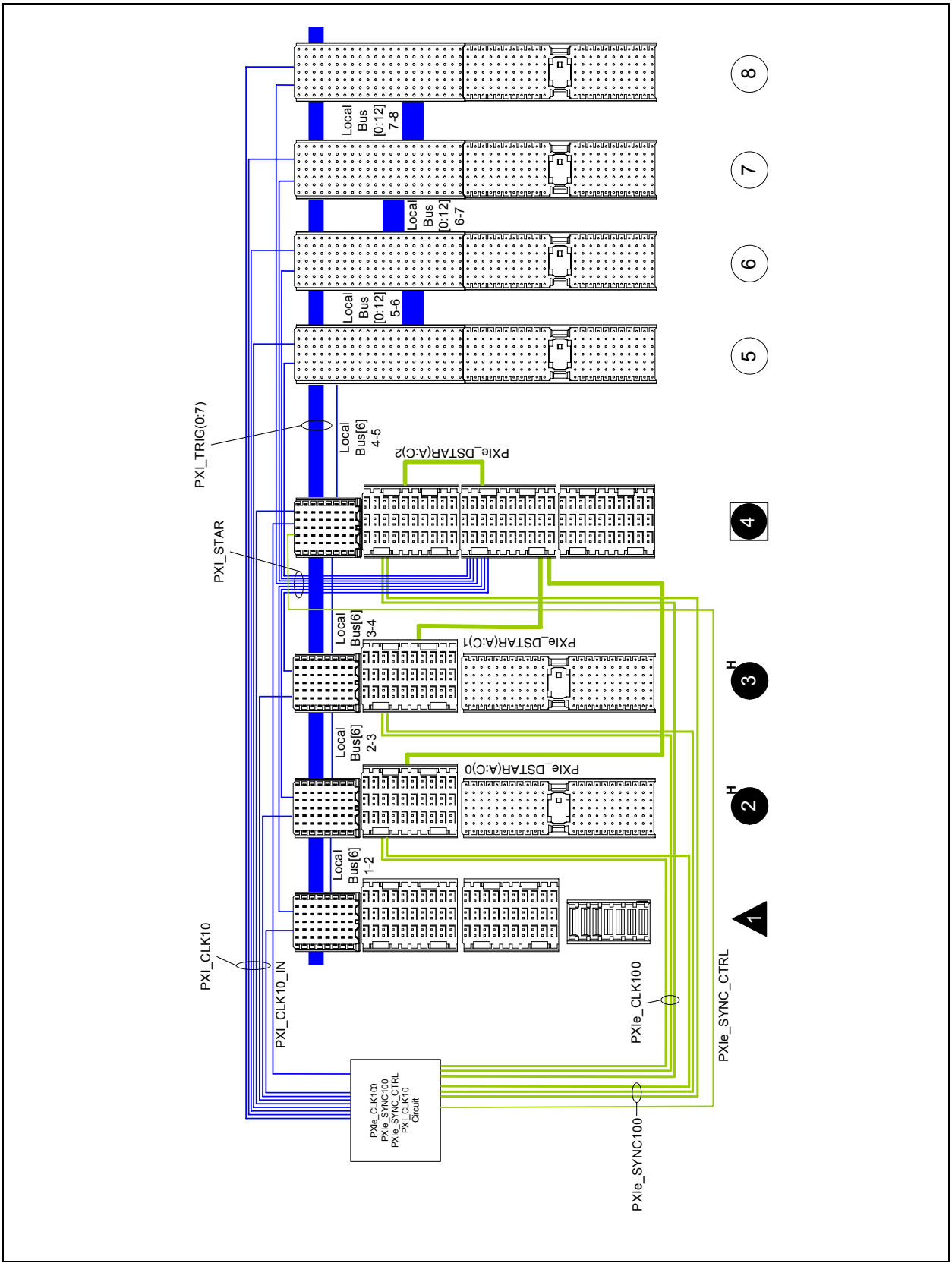

Figure 2-19. Instrumentation Signal Implementation Example

Figure 2-20 shows how the instrumentation signals are mapped to the connectors of the Hybrid Slot, PXI Express Peripheral Slot, and the System Timing Slot.

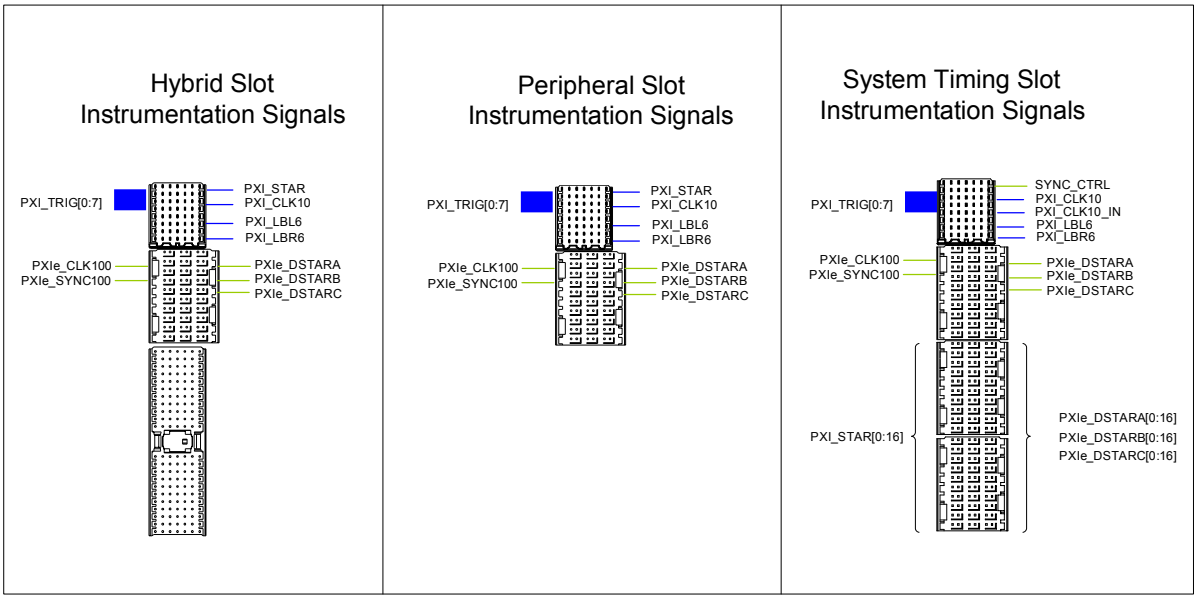

Figure 2-20. Instrumentation Signals Connector Mapping

2.2.3.1 High-Frequency System Reference Clock

The High-Frequency System Reference Clock, or PXIe_CLK100 as it is called out in the specification, is the most significant addition for timing in PXI Express. This signal provides a differential, 100 MHz LVPECL clock to each PXI Express Peripheral Slot in the system. Advancing technology has allowed PXI to adopt differential clocking, which provides for increased noise immunity in the backplane. This allows instrumentation Modules to receive a clock with low jitter and improve overall system performance. The differential technology also allows for a higher frequency reference clock of 100 MHz. This not only allows for higher performance clocking, but also allows the cost of Modules to be lowered by eliminating clock multiplication for Modules able to work with PXIe_CLK100 and divisions directly. The PXIe_CLK100 is added into the specification in a way to be completely interoperable with PXI_CLK10. The PXI_CLK10 and PXIe_CLK100 are phase aligned and allow for highly accurate synchronization of devices, including all PXI-1 compliant devices, no matter which clock is used.

2.2.3.2 Differential Synchronization Signal

With the High-Frequency System Reference Clock (PXIe_CLK100) comes the need to accurately synchronize Modules using this reference clock along with those using PXI_CLK10. The Differential Synchronization Signal or PXIe_SYNC100 is routed by the backplane to each Module and provides this capability. This signal is synchronous to PXIe_CLK100 and asserts one out of every 10 clocks to indicate the phase relationship of the 10 MHz and 100 MHz reference clocks. This is key for synchronization and triggering in that it allows the existing triggering capabilities to be used and interoperate. Devices using the Trigger Bus can send triggers synchronous to PXI_CLK10 no matter what system reference clock is used. The PXIe_SYNC100 also provides a synchronization signal for Modules wanting to divide the 100 MHz reference clock for use on the Module. This allows multiple Modules to begin the clock division on the same clock edge without requiring a high-frequency trigger bus.

2.2.3.3 Differential Triggers

Previous PXI specifications could take advantage of the low cost of TTL logic to provide a complete timing and synchronization system. While TTL logic provided efficient implementations, it does come with a limit on the frequencies that may be transmitted in the system. With PXI Express, the clocking and triggering system can take advantage of the lowered cost of differential signaling and provide high-quality and high-frequency connections to each Module. In the same way that PXI_STAR allows a direct connection between each Module to a central timing resource, the Differential Star Triggers allows for three direct, high-frequency connections back to the System Timing Module. A key benefit of these signals is the ability to transmit high-frequency, high-quality clocks to and from Modules in a PXI system. By having multiple connections, a larger number of system applications may be solved by providing increased routing capabilities. While a primary application of PXIe_DSTAR will be clock distribution, the signals are flexible and allow for a large number of unique applications of these connections.

2.2.3.4 System Timing Module

The Slot 2 or Star Trigger Slot of PXI-1 provides access to advanced system timing applications with individual connections to each Module and the ability to replace the system clock reference. With the addition of the Differential Star Triggers and High-Frequency System Reference Clock, a larger number of high-performance connections are required to be provided by the backplane to the Modules. The System Timing Module (STM) is the connection point for the three starred signals added to each Module. The STM becomes the central connection point and routing manager for the most advanced timing and synchronization capabilities for a PXI Express system. The System Timing Module in PXI Express Systems replaces the Star Trigger Module defined in PXI-1 while it retains the connection point for PXI_STAR to each Module and it provides the connection point for clock replacement in the backplane. The STM is also key in providing the access to support highly synchronized systems across multiple Chassis of heterogeneous systems. While backplanes will provide the capability to support an STM, the System Timing Slot (STS) may accept a PXI Express Peripheral Module if the advanced timing synchronization capabilities are not necessary in a system.

2.2.4 Slot Identification

PXI Express has explicit hardware support for geographical addressing. A PXI Express device can determine its slot number by reading the GA(4:0) pins. Previously, to create the `pxisys.ini` file describing the topology of the PXI system, a PXI resource manager needed to use the run time PCI device tree, the `chassis.ini` files, and vendor-specific information about the PCI topology of the Slot 1 Controller. Using the new hardware support, a full PCI bus tree is no longer needed. Each Module can discover its slot number independently.

2.2.4.1 Module Drivers and the GA Pins

For instrument drivers, VISA implementations, and application software to find a particular device by slot number, the driver for each Module must provide a mechanism to report its slot number to other software components in the system. This mechanism is defined in the PXI-6: *PXI Express Software Specification*.

2.2.4.2 Determining the Chassis Number

Although there is explicit hardware support for determining a Module's slot number, the mechanism for determining a Chassis number requires knowledge of the bus and device numbers of some of the PCI Express Switches and of the Modules in the system. The PXI Express Software specification describes the interfaces for discovering the Chassis number for a PXI Express Module.

2.2.5 Controller Identification

PXI Express has hardware support for identification of a PXI Express Chassis using an EEPROM on the SMBus. PXI Express also uses information about the bus numbers of the links from the system Module to the Chassis to enumerate which devices are in which Chassis. Therefore, the *PXI Express Software Specification* defines a mechanism for identifying what Controllers exist, how those Controllers access the SMBus, and what bus numbers are subordinate to that Controller.

The *PXI Express Software Specification* specifies an interface for accessing the SMBus using a Slot 1 Controller. There is a one-to-one correspondence between Slot 1 Controllers and instances of the PXI Express SMBus Controller interface.

2.2.6 Chassis Identification

PXI Express leverages the requirements set in the CompactPCI Express specification for the Backplane Identification and Capability EPROM. This EPROM is accessed by the system Module via the SMBus and gives the PXI Express system a way to uniquely identify the vendor, model, revision, and serial number of the Chassis. It also provides information on the slots within the Chassis and the PCI Express topology. This information can be used by software to load a Chassis driver to provide additional information about the Chassis or access backplane and Chassis functionality.

2.2.7 Power Requirements

The power requirements for PXI Express systems include the following defined in CompactPCI Express:

- Power rails
- Current capacity of the power pins for a slot
- Regulation
- Ripple and noise
- Decoupling
- Power rail timing
- Power supply signals to and from the system Module

PXI Express additionally includes Chassis power supply minimum current requirements per voltage rail for each slot type. This guarantees a high level of interoperability between Modules and Chassis and gives guidance to PXI Express Module designers on how much current they can expect from a Chassis. Power requirements for PXI-1 slots implemented in PXI Express systems are defined in the PXI-1 Specification.

2.3 Software Architecture Overview

PXI Express introduces new software features for managing the new hardware features of CompactPCI Express and PXI Express. These new features include:

- A software interface for accessing SMBus devices, such as the serial EEPROM of each Chassis.
- A software interface for accessing the slot number of each Module as provided by the GA pins.
- A mechanism for associating a Chassis number with the Modules in each Chassis.
- A software protocol for enumerating PXI components, such as Controllers, Modules, Chassis, and other resources.
- A namespace for those PXI components.
- A general registration mechanism for services implemented by the drivers for PXI components.
- Standard software interfaces for services implemented by Controllers, Chassis and Modules.

The *PXI Express Software Specification* requires each Controller, Chassis, and Module to include software implementing certain services, and to register those services. By creating standards for these services and how they are registered, the *PXI Express Software Specification* provides a new level of interoperability. If, for example, a Controller, a Chassis, a Module, and a VISA implementation are each provided by a different vendor, all of the following are possible:

- The VISA implementation can determine the physical location of the Module by interacting with the Module driver.
- The Chassis driver can control backplane resources by using the SMBus driver on the Slot 1 Controller.
- A configuration tool can determine the list of Chassis and Modules in the system.

The new software requirements and features for PXI Express are specified in the *PXI Express Software Specification*.

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3. Mechanical Requirements

This section defines the mechanical requirements for PXI Express systems. It discusses the maximum number of slots, the location of the system slot, slot numbering, PXI-1 slots, Chassis requirements, connector requirements, Module types, the interoperability of the Controller with the Chassis, the PXI Express logo/glyphs, environmental testing, and cooling.

3.1 Drawing Standard

The drawings in this specification shall be interpreted per ANSI Y14.100.

3.2 Dimensional Units

Dimensions in this specification are in millimeters unless otherwise specified.

3.3 Chassis Subrack Mechanical Requirements

RULE: Just as with PXI-1, CompactPCI, and CompactPCI Express, a PXI Express Chassis SHALL use PICMG 2.0-compliant Chassis Subracks.

3.4 Minimum Slot Requirements to be a PXI Express Chassis

RULE: A PXI Express Chassis SHALL at least have either one PXI Express Peripheral Slot or one Hybrid Slot.

RULE: A PXI Express Chassis SHALL NOT have a Star Trigger Slot as defined in the PXI-1 Specification.

RECOMMENDATION: A PXI Express Chassis SHOULD have a System Timing Slot.

3.5 Features Leveraged from PXI-1: PXI Hardware Specification

3.5.1 Maximum Number of Slots

Since the CompactPCI Express specification accommodates 31 slots based on the definition of the Geographical Addressing pins, it is necessary to limit a PXI Express Chassis to 31 slots.

RULE: A PXI Express Chassis SHALL NOT have more than 31 slots.

3.5.2 System Slot Location and Rules

All PXI Express-compatible systems require a backplane/Chassis, a System Timing Slot, and at least either one PXI Express Peripheral Slot or one Hybrid Slot. A System Slot is not a requirement if the system Module functionality is built into the Chassis. If the Chassis does have a System Slot, it allows users to mix and match different Controllers. However, because the CompactPCI Express specification allows a System Slot to be located anywhere relative to Peripheral Slots, the possibility for confusion and incompatibility exists. To address this problem the following rules must be followed for PXI Express-compatible systems:

RULE: The System Slot SHALL be defined as the leftmost PXI slot in a PXI Chassis/backplane. For documentation purposes, this slot is counted as one *System* Slot.

RECOMMENDATION: If the System Module requires more than one slot width, it SHOULD extend to the LEFT of the System Slot in full slot increments (one slot equals 20.32 mm, or 0.8 in.) into additional Controller expansion slots.

OBSERVATION: In a PXI Express system, these additional Controller slots are for physical expansion of the System Controller Module only and cannot support Peripheral Modules. These slots DO NOT have connectors that interface to PCI Express links routed on the backplane.

OBSERVATION: Extending the System Module to the LEFT allows all PXI Express Peripheral Slots to be used.

RECOMMENDATION: The System Module SHOULD NOT extend to the RIGHT of the System Slot into Peripheral Slots.

OBSERVATION: If a System Module expands to the right, the number of usable PXI Express Peripheral Slots may be compromised.

RULE: Every PXI Express System Module SHALL clearly document how many Controller expansion slots (to the left of the System Slot) and Peripheral Slots it occupies.

RULE: Every PXI Express Chassis SHALL clearly document how many Peripheral and Controller Expansion Slots are available.

OBSERVATION: The two preceding rules help ensure that end users can easily determine whether a particular Controller-Chassis pair is compatible and how many Peripheral Slots are available.

Figure 2-17 depicts typical System Expansion Slot designations in a PXI Express System.

3.5.3 Slot Numbering and Orientation

PXI Express Chassis slot numbering is handled the same way that the PXI-1 Specification requires. The exception is that PXI Express allows for Chassis that have the System Module to be built in.

RULE: PXI Express Chassis with a System Slot SHALL meet the slot numbering requirements set in the PXI-1 Specification.

RULE: PXI Express Chassis without a System Slot (the System Module is built in), SHALL meet the slot numbering requirements set in the PXI-1 Specification, except the slots will have their numbering begin at the number 2.

PERMISSION: Slot orientation and numbering schemes other than those defined in PXI-1 MAY be used as long as it is clear and logical for the end user.

3.5.4 PXI-1 Slot

In a PXI Express Chassis, there may be slots that support PXI boards as they are defined in PXI-1 (*PXI Hardware Specification*, Revision 2.2). These slots meet the mechanical requirements of the *PXI Hardware Specification* and are referred to as PXI-1 slots.

PERMISSION: PXI-1 3U and 6U Peripheral Modules and Slots are MAY be used in PXI Express Systems.

RULE: PXI-1 slots in a PXI Express Chassis SHALL meet the mechanical requirements set in the PXI-1 Specification.

RULE: PXI-1 Peripheral Modules SHALL NOT be plugged into Hybrid Peripheral Slots unless they meet the requirements for Hybrid Slot Compatible PXI-1 Modules as defined by this specification.

RECOMMENDATION: PXI-1 3U and 6U Peripheral Modules SHOULD also meet the side-2 component height recommendation as defined by the CompactPCI Express specification to minimize mechanical interference issues.

3.5.5 Hybrid Slot-Compatible PXI-1 Peripheral Modules

PXI-1 or an associated ECN defines a 3U and 6U Hybrid Slot Compatible PXI-1 Peripheral Module that consists of a 3U or 6U PXI-1 Module where the J2 HM connector has been replaced with an eHM connector. The eHM connector is a modified 2 mm HM connector that includes application keying and is installed in the same location as the upper eight columns of the PXI-1 J2 connector. This board type may be used in any PXI-1 or PXI Express Hybrid Slot.

OBSERVATION: A Hybrid Slot Compatible PXI-1 Peripheral Module MAY be used in a legacy PXI-1 or PXI Express Hybrid Slot.

3.6 Features Leveraged from CompactPCI Express Specification

Just as PXI-1 was based on CompactPCI, PXI Express is based on CompactPCI Express, which has integrated PCI Express into a CompactPCI type architecture. This section outlines the features rules, suggestions, permissions, and observations leveraged from that specification.

RULE: All mechanical requirements defined by the CompactPCI Express specification SHALL be met unless stated otherwise in this specification.

3.6.1 Module Connector Requirements

3.6.1.1 Advanced Differential Fabric (ADF) Connector

RULE: PXI Express Modules SHALL use the ADF-F-3-10-2-F-25 connector as defined by the CompactPCI Express specification.

3.6.1.2 Enriched Hard-Metric (eHM) Connector

RULE: PXI Express Modules SHALL use the eHM-F2 connector as defined by the CompactPCI Express specification.

3.6.1.3 Universal Power (UPM) Connector

RULE: System Controller Modules SHALL use the UPM-M-7 or UPM-M-7-HP connector as defined by the CompactPCI Express specification.

3.6.2 Backplane Connector Requirements

3.6.2.1 Advanced Differential Fabric (ADF) Connector

RULE: PXI Express Slots SHALL use the ADF-M-3-10-2-B-25 or ADF-M-3-10-2-S-25-0100 connector as defined by the CompactPCI Express specification.

3.6.2.2 Enriched Hard-Metric (eHM) Connector

RULE: PXI Express Slots SHALL use the eHM-M2-HP or eHM-M2 connector as defined by the CompactPCI Express specification.

3.6.2.3 Universal Power (UPM) Connector

RULE: System Controller Slots SHALL use the UPM-F-7 connector as defined by the CompactPCI Express specification.

3.6.3 3U and 6U Module Requirements

3.6.3.1 System Module

RULE: 3U and 6U PXI Express Modules SHALL meet the mechanical requirements as defined in the CompactPCI Express specification.

OBSERVATION: 6U PXI Express System Modules and backplanes MAY use J3/P3, J4/P4, and J5/P5 if desired for rear I/O applications.

3.6.3.2 PXI Express Peripheral Module

RULE: The 3U PXI Express Peripheral Modules SHALL meet the mechanical requirements for the 3U Type 2 Peripheral Module as defined in the CompactPCI Express specification.

RULE: The 6U PXI Express Peripheral Modules SHALL meet the mechanical requirements for 6U Type 2 Peripheral Boards as defined in the CompactPCI Express specification with the exception that the J3/J4/J5 connectors SHALL NOT be used. The 6U PXI Express Peripheral Module PCB SHALL meet the requirements defined by Figure 3-1.

RULE: 6U PXI Express Peripheral Modules that are not 6U System Timing Modules SHALL NOT have any connectors other than the XJ3, XJ4, and XJ8 connectors.

PERMISSION: 6U PXI Express Peripheral Modules MAY populate the Optional eHM connector, in the XJ8 position as shown in Figure 3-1, when additional power is required.

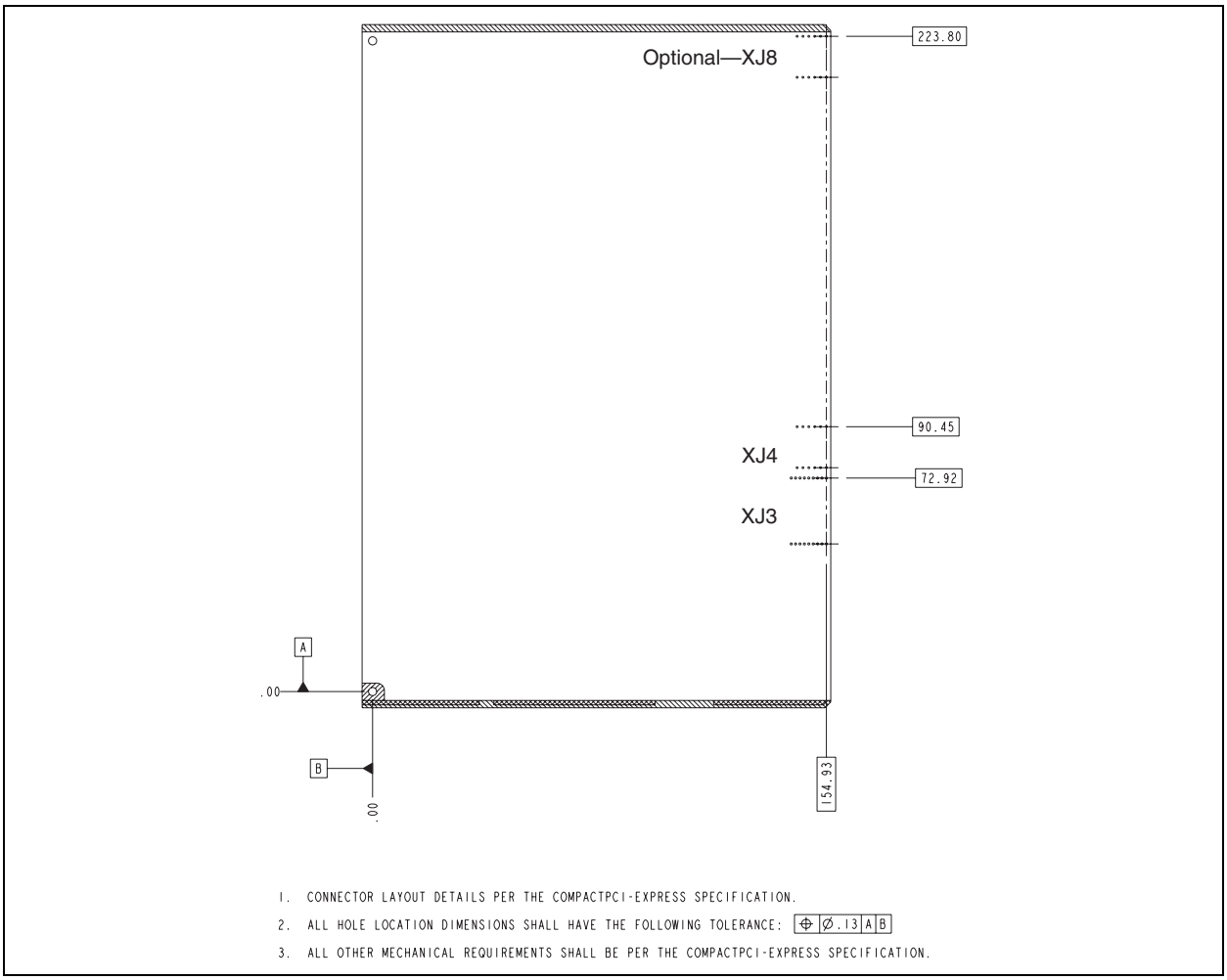

Figure 3-1. 6U PXI Express Peripheral Module PCB

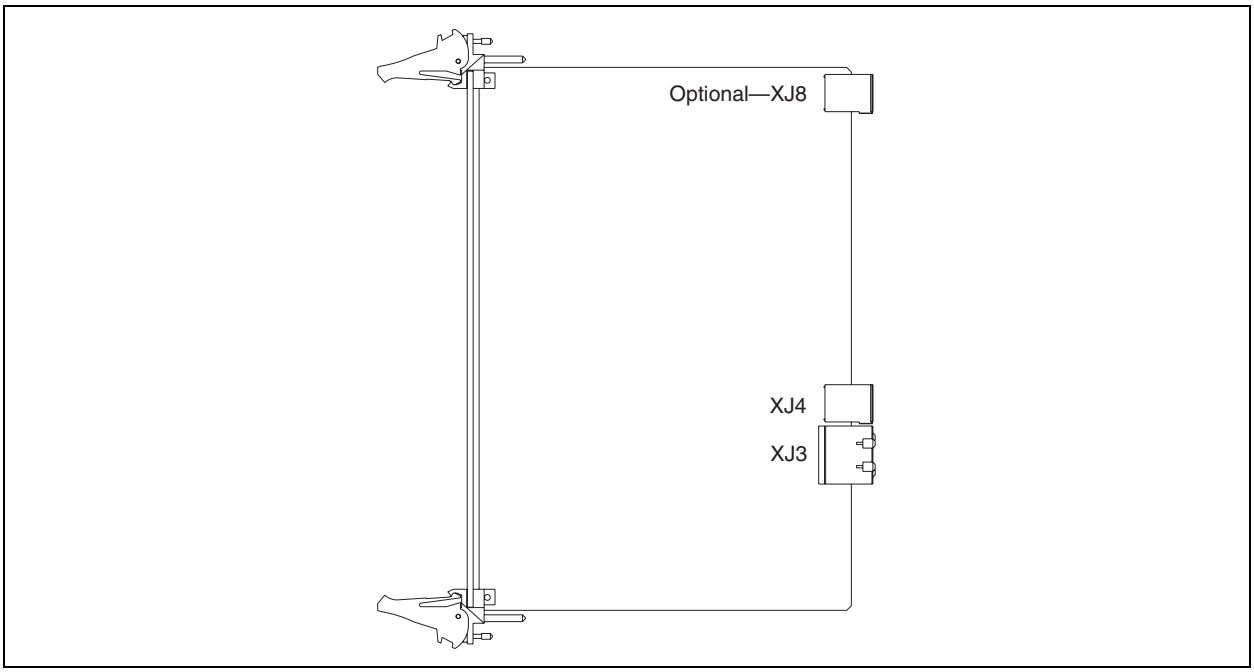

Figure 3-2. 6U PXI Express Peripheral Module

3.6.4 Backplane Requirements

RULE: 3U and 6U PXI Express backplanes SHALL meet the size, mechanical mounting hole, and tolerance requirements as defined in the CompactPCI Express specification.

Requirements for the various connector locations are defined in further detail in the following sections.

3.6.4.1 System Slot

RULE: 3U and 6U PXI Express System Slots SHALL meet the mechanical requirements defined in the CompactPCI Express specification.

PERMISSION: As with CompactPCI Express, 6U System Slots MAY use J3/J4/J5 if desired for rear I/O applications.

3.6.4.2 Peripheral Slot

RULE: 3U PXI Express Peripheral Slots SHALL meet the mechanical requirements for 3U Type 2 Peripheral Slots as defined in the CompactPCI Express specification.

RULE: 6U PXI Express Peripheral Slots SHALL meet the mechanical requirements for 6U Type 2 Peripheral Slots as defined in the CompactPCI Express specification with the exception that an additional XP8 eHM connector SHALL be populated in the location shown in Figure 3-3.

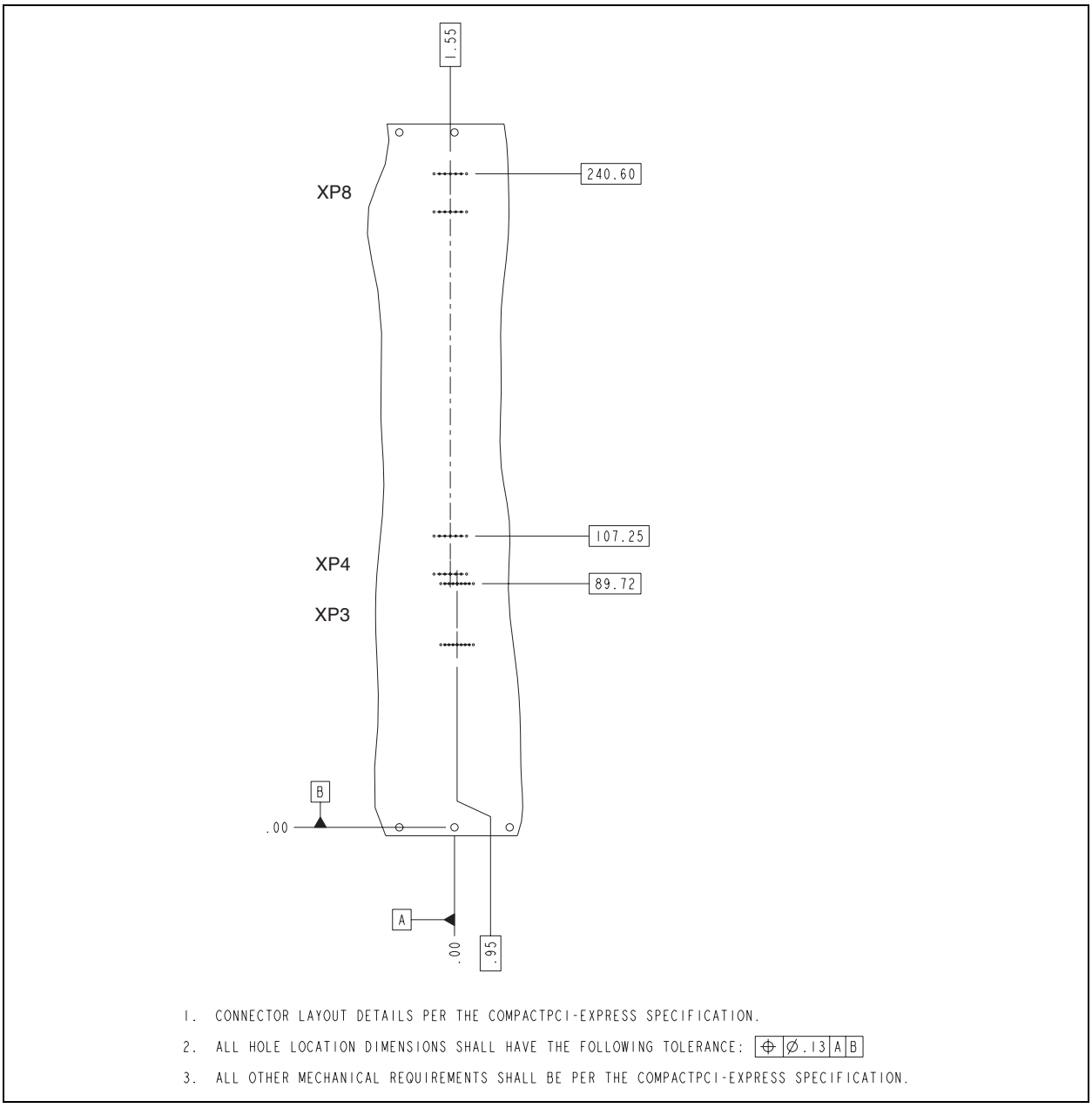

Figure 3-3. 6U PXI Express Peripheral Slot

3.6.4.3 PXI Express Hybrid Peripheral Slot

RULE: 3U PXI Express Hybrid Peripheral Slots SHALL meet the mechanical requirements for 3U Hybrid Peripheral Slots as defined in the CompactPCI Express specification.

RULE: 6U PXI Express Hybrid Peripheral Slots SHALL meet the mechanical requirements for 6U Hybrid Peripheral Slots as defined in the CompactPCI Express (PICMG EXP.0) specification, with the exceptions that the XP8 eHM connector SHALL be populated in the position shown in Figure 3-4, and the legacy P3/P4/P5 connectors SHALL NOT be used.

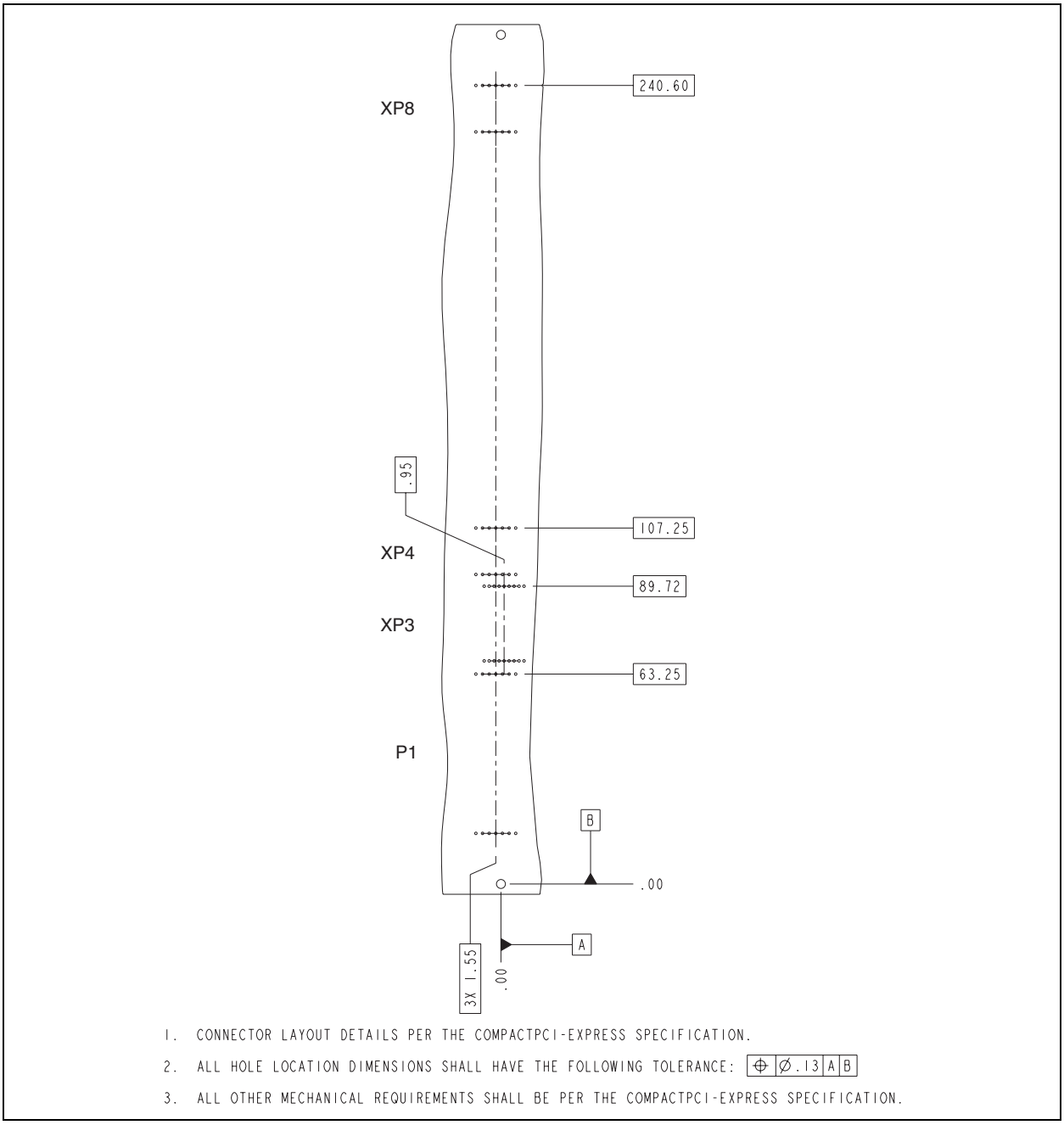

Figure 3-4. 6U PXI Express Hybrid Slot

3.7 New Module and Slot Types

3.7.1 PXI Express System Timing Module Requirements

RULE: 3U PXI Express System Timing Modules SHALL meet the mechanical requirements as defined in Figure 3-5.

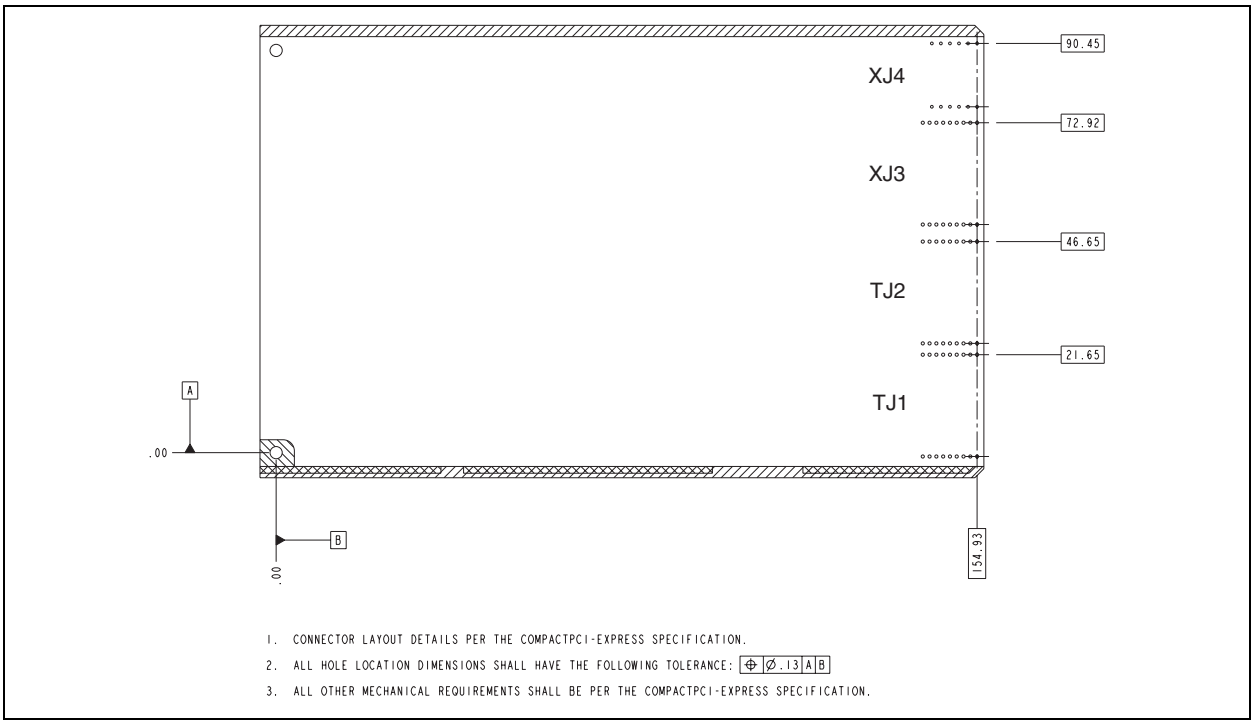

Figure 3-5. 3U PXI Express System Timing Module PCB

RULE: 6U PXI Express System Timing Module PCBs SHALL meet the mechanical requirements as defined in Figure 3-6.

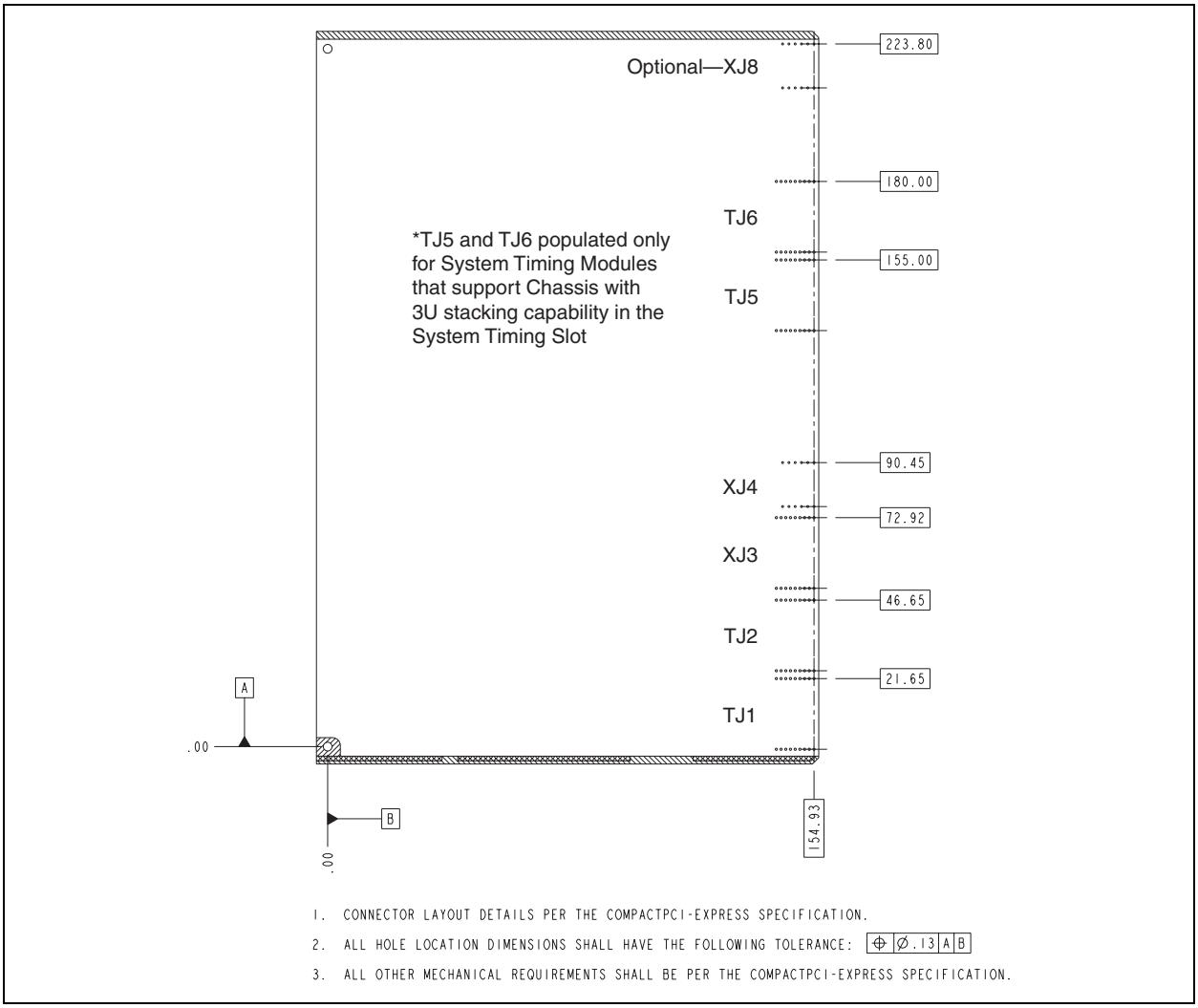

Figure 3-6. 6U PXI Express System Timing Module PCB

PERMISSION: A 6U PXI Express System Timing Module MAY populate TJ5 and TJ6 connectors to allow it to be used in a Chassis that requires such a Module to provide enough star triggers or differential triggers, or in a Chassis that supports stacking 3U System Timing Modules.

3.7.2 Backplane Requirements for New Slot Types

RULE: 3U and 6U PXI Express backplanes SHALL meet the size, mechanical mounting hole, and tolerance requirements as defined in the CompactPCI Express specification.

Requirements for the various connector locations are defined in further detail in the following sections.

3.7.2.1 PXI Express System Timing Slot Requirements

RULE: 3U PXI Express System Timing Slots SHALL meet the mechanical requirements as defined in Figure 3-7.

RULE: 6U PXI Express System Timing Slots SHALL meet the mechanical requirements as defined in Figure 3-8.

RULE: 6U PXI Express System Timing Slots that support stacking 3U System Timing Modules SHALL meet the mechanical requirements as defined in Figure 3-9.

RULE: If the TP1 connector is not populated on a System Timing Slot, there SHALL be a 2.2 mm maximum component height restriction zone on the backplane where the TP1 connector would normally be to avoid interference with System Timing Modules that have TJ1 populated.

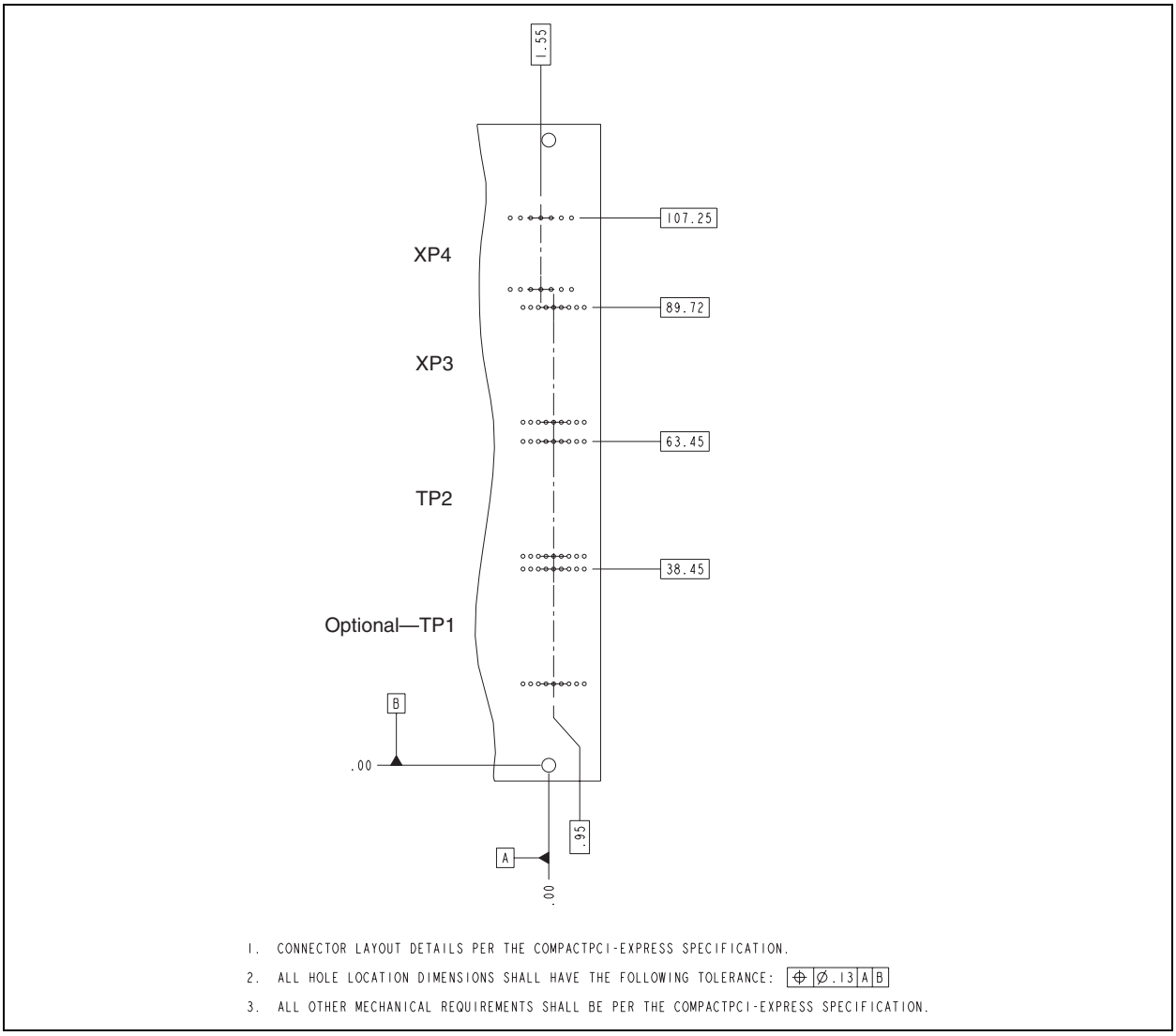

Figure 3-7. 3U PXI Express System Timing Slot Backplane Dimensions

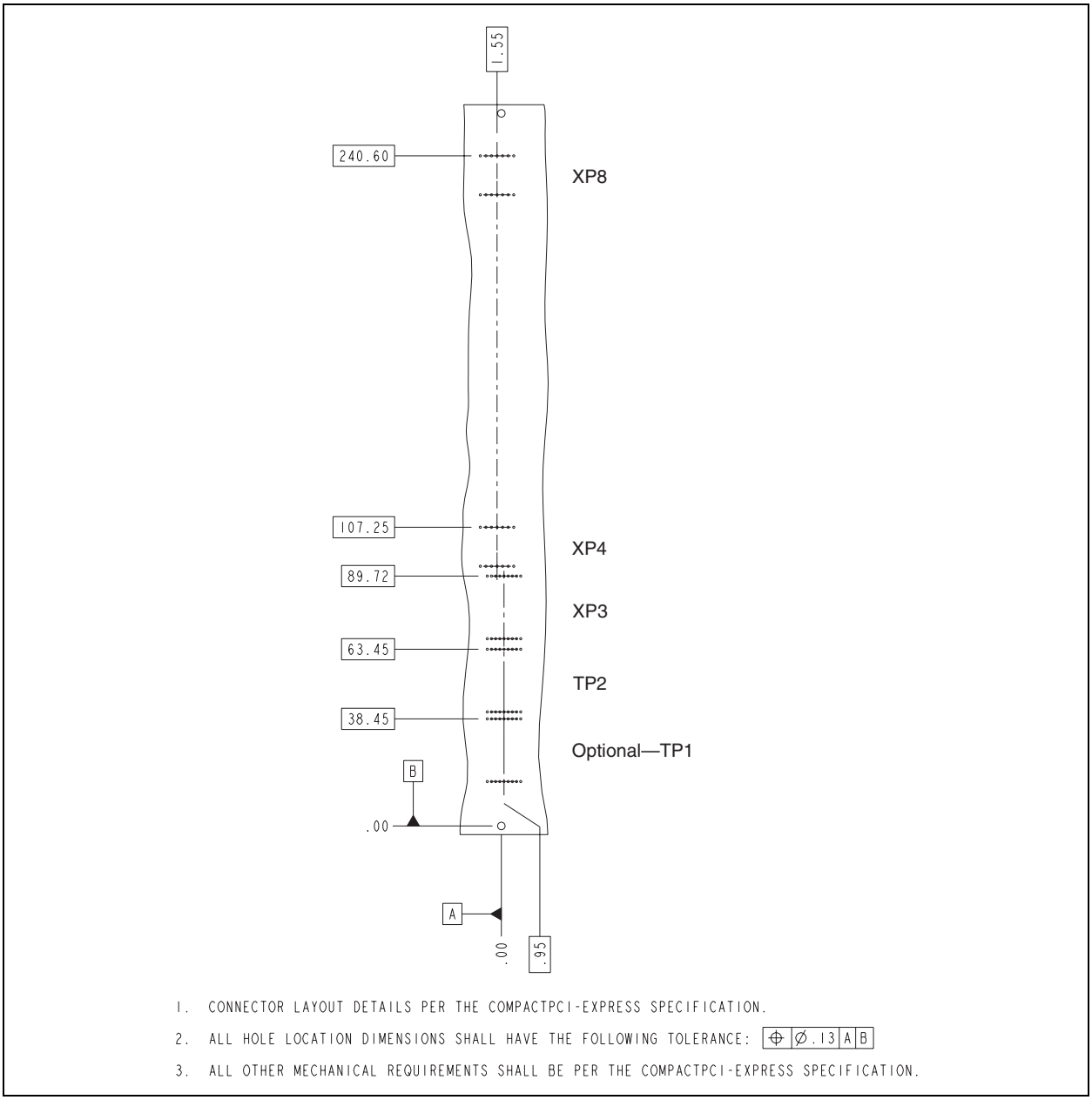

Figure 3-8. 6U PXI Express System Timing Slot Backplane Dimensions

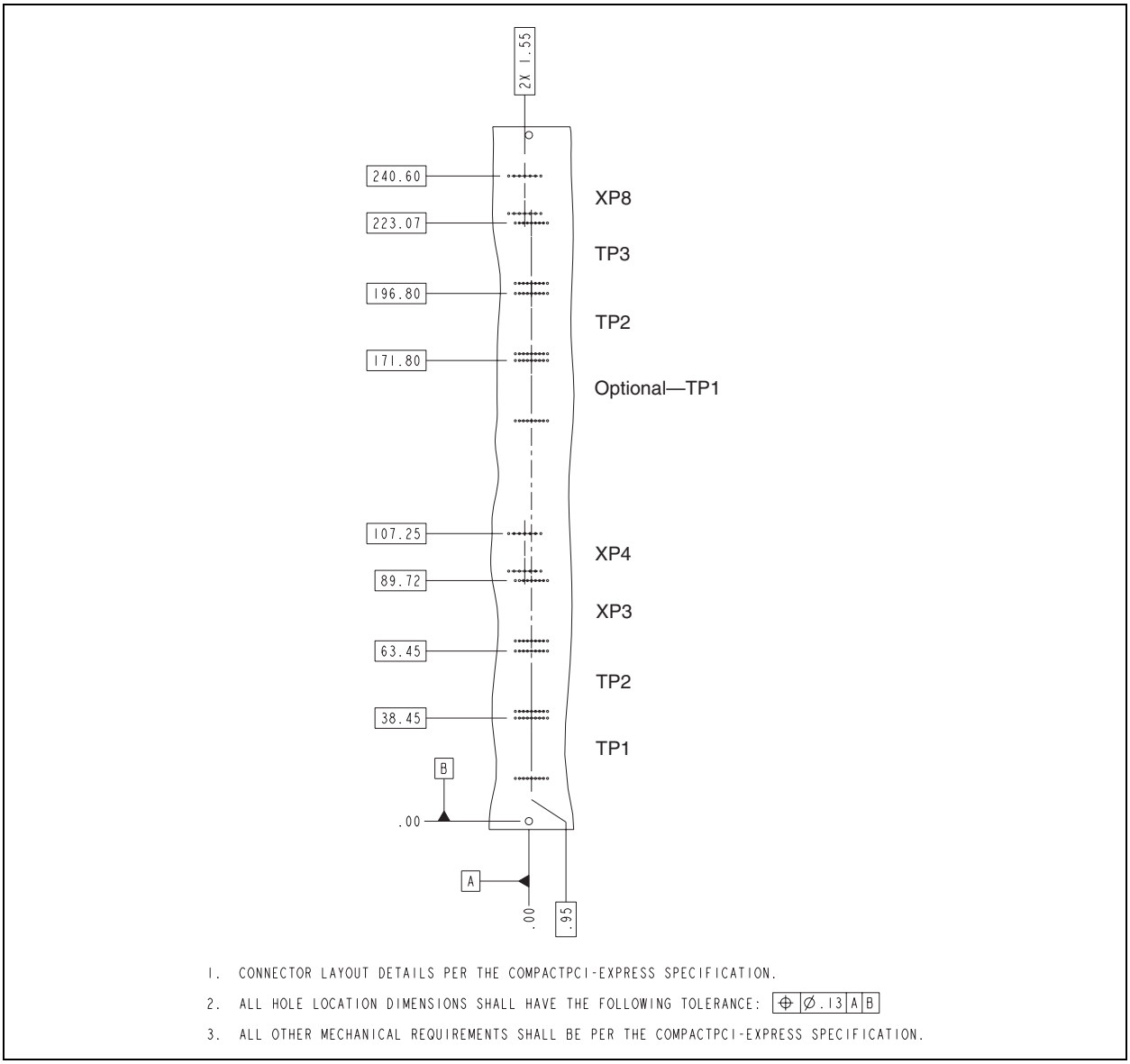

Figure 3-9. 6U PXI Express System Timing Slot with Stacked Support Backplane Dimensions

RULE: For applications where the backplane TP1 connector is Optional, there SHALL be a 2.2 mm max high component keep out region on the backplane in the TP1 area to avoid interference with timing Modules that have TJ1 populated.

PERMISSION: If a 3U PXI Express backplane can connect all slots that can connect to star triggers and differential triggers via the TP2 connector, the TP1 connector MAY NOT be populated.

PERMISSION: A 6U PXI Express backplane, to provide enough differential triggers and star triggers to all slots that can connect to them, could support either stacking two 3U System Timing Modules or a 6U System Timing Module with additional connectors. If such a 6U PXI Express backplane can connect all slots that can connect to star triggers and differential triggers without using the TP5 connector, the TP5 connector MAY NOT be populated.

3.8 Requirements for Stacking 3U Modules in 6U Slots

Just as with the PXI-1 specification, PXI Express allows for efficient use of 3U Modules in a 6U Chassis.

Mechanically, this configuration can be accomplished by making use of center extrusions fixed within the Chassis to physically support the insertion, extraction, and mounting of the lower and upper 3U Modules residing in a 6U Slot. Alternatively, this may accomplished mechanically by a stacking adapter attached to the two 3U Modules prior to insertion into the 6U Slot. Figure 2-18 shows an example of a 6U Chassis that supports stacking 3U Modules.

RULE: 6U PXI Express Chassis that support stacking 3U Modules SHALL populate the appropriate connectors in the lower half of the 6U Slot to implement a lower 3U Slot according to the type of 3U Slot being implemented (System, Hybrid, PXI Express Peripheral, PXI-1, or System Timing Slot).

RULE: 6U PXI Express Chassis that support stacking 3U Modules SHALL populate the appropriate connectors in the upper half of the 6U Slot to implement an upper 3U Slot according to the type of 3U Slot being implemented (Hybrid, PXI Express Peripheral, PXI-1, or System Timing Slot).

RULE: Table 3-1 shows the upper 3U Slot that SHALL and SHALL NOT be implemented based on how the lower 3U Slot is implemented within a 6U Slot of a PXI Express Chassis that supports stacking 3U Modules.

Table 3-1. Upper and Lower 3U Slot Implementation

	Upper 3U Slot				
Lower 3U Slot	**System**	**PXIe Peripheral**	**System Timing**	**Hybrid Peripheral**	**PXI 2.X Peripheral**
System	No	Yes	No	Yes	Yes
PXIe Peripheral	No	Yes	No	Yes	No
System Timing	No	Yes	Yes	No	No
Hybrid Peripheral	No	Yes	No	Yes	No
PXI 2.X Peripheral	No	Yes	No	Yes	Yes

OBSERVATION: An upper 3U System Timing Slot is not allowed above any slot other than the lower 3U System Timing Slot.

OBSERVATION: Upper 3U System Slots are not allowed.

OBSERVATION: A lower slot that is a PXI Express Peripheral Slot, System Timing Slot, or a Hybrid Peripheral Slot cannot have a PXI-1 Peripheral Slot in the upper position. This is so a 6U Module can have the upper eHM connector for extra power and still plug into 6U Slots that support stacking 3U Modules.

3.9 PXI Logo

PXI Express products use the same logo as PXI products. PXI Express Peripheral Modules, PXI Express System Modules, PXI Express System Timing Modules, and PXI Express Chassis may have the PXI Express logo on their marketing material, datasheets, and manuals to help customers identify that the PXI products have PCI Express capabilities.

PERMISSION: Vendors who are members of the PXI Systems Alliance MAY use the PXI logo as defined below on either the front panel or the injector/ejector handle of products claiming full compliance with the *PXI Express Hardware Specification*.

RULE: If the PXI logo is used, the vendor SHALL obtain a license to use the trademarked logo from the PXI System Alliance.

RULE: If the PXI logo is used, it SHALL NOT be altered in any way other than scale. The logo SHALL NOT incorporate any additions.

Figure 3-10 shows the PXI logo. PXI Systems Alliance members can obtain logo artwork and the license from the alliance.

Figure 3-10. PXI Logo

RULE: Vendors who are members of the PXI Systems Alliance SHALL NOT use the PXI Express logo as defined below on any part of PXI or PXI Express hardware products.

PERMISSION: Vendors who are members of the PXI Systems Alliance MAY use the PXI Express logo as defined below in the marketing material, datasheets, and manuals of PXI Express Peripheral Modules, PXI Express System Modules, PXI Express System Timing Modules, and PXI Express Chassis claiming full compliance with the *PXI Express Hardware Specification*.

RULE: If the PXI Express logo is used, the vendor SHALL obtain a license to use the trademarked logo from the PXI System Alliance.

RULE: If the PXI Express logo is used, it SHALL NOT be altered in any way other than scale. The logo SHALL NOT incorporate any additions.

Figure 3-11 shows the PXI Express logo. PXI Systems Alliance members can obtain logo artwork and the license from the alliance.

Figure 3-11. PXI Express Logo

3.10 Chassis with Built-In System Modules

PERMISSION: A PXI Express Chassis MAY have a built-in System Module and therefore not have a System Slot.

3.11 Cooling Requirements

3.11.1 Module Cooling Requirements

RULE: Modules SHALL be designed to allow a suitable airflow path from bottom to the top of the Module as shown in Figure 3-12.

OBSERVATION: Airflow, and thus cooling, through a Module depends on the Chassis as well as the Module design. Modules with a lower airflow resistance will receive more airflow, and those with higher resistance will receive less air flow for a given Chassis.

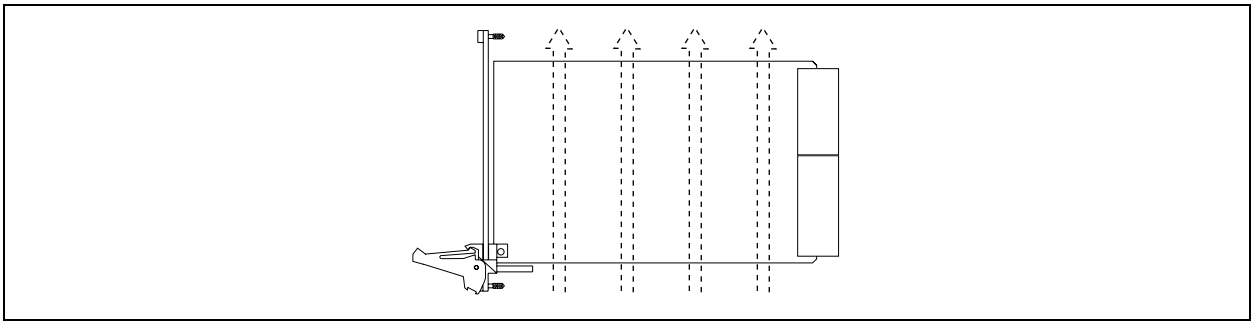

Figure 3-12. Cooling Airflow Direction in a PXI Express System

RULE: Module manufacturers SHALL document and make available to the customer the nominal and peak power dissipated by the Module, by voltage rail, under normal operating conditions.

RECOMMENDATION: Single-width 3U Modules SHOULD NOT dissipate more than 30 W within the Chassis.

RECOMMENDATION: Single-width 6U Modules SHOULD NOT dissipate more than 60 W within the Chassis.

OBSERVATION: 6U Chassis typically require more airflow per slot than a 3U Chassis for a given ambient temperature specification due to preheating effects

3.11.2 Chassis Cooling Requirements

RULE: Chassis SHALL provide forced airflow that flows from the bottom to the top of a Module as shown in Figure 3-12.

OBSERVATION: For typical Chassis configurations, the airflow through a slot will be flowing against gravity or upwards, (that is, in the same directly of naturally rising hot air). This specification does not, however, preclude other Module orientations such as horizontal.

RULE: Chassis manufacturers SHALL document and make available to the customer the maximum total power that a given Chassis can dissipate within the Subrack and the maximum power it can dissipate for the worst-case slot. Furthermore, the manufacturer SHALL document and make available to the customer the specific test procedure used to determine these power dissipation levels.

RECOMMENDATION: The worst-case slot power dissipation value SHOULD be based not only on how much power may be available to a given slot, but also on the cooling capabilities of the Chassis for the worst-case slot.

RECOMMENDATION: Thermal load cards SHOULD be used in all Chassis slots while determining the cooling capabilities for the Chassis and the worst slot.

RULE: PXI Chassis SHALL have filler panels installed in slots that do not have Modules populated.

OBSERVATION: If filler panels are not installed in slots that do not have populated Modules, proper Module cooling cannot be guaranteed.

3.12 Environmental Specifications

RECOMMENDATION: The environmental testing listed below SHOULD be carried out according to the procedures described in IEC 60068.

RULE: Test results and reports generated for environmental testing SHALL be made available to end users of PXI Express Systems. All manufacturers of PXI Express Chassis and Modules SHALL supply the required environmental ratings, as described below, for their products.

RECOMMENDATION: All manufacturers SHOULD provide the required environmental ratings, as described below, in their product datasheets.

RULE: If a manufacturer chooses to use environmental testing procedures other than those recommended above, these procedures, in addition to the test results and reports, SHALL be documented and made available to the customer.

OBSERVATION: It is the system integrator's responsibility to select Modules and Chassis appropriate for the application's environmental requirements.

3.12.1 Temperature Specifications

RULE: PXI Chassis and Modules SHALL be tested for storage and operating temperature ranges.

3.12.2 Humidity Specifications

RECOMMENDATION: PXI Express Chassis and Modules SHOULD be tested for humidity.

3.12.3 Vibration Specifications

RECOMMENDATION: PXI Express Chassis and Modules SHOULD be tested for vibration.

3.12.4 Acoustic Noise Specifications

RECOMMENDATION: All PXI Express Chassis SHOULD be tested for acoustic noise levels (A-weighted sound pressure level, L_{PA}). This acoustic testing SHOULD be carried out according to ISO-7779 on a standard test table at the operator position. Chassis testing SHOULD be conducted with the Chassis running at full load with front panels installed. If multiple fan speed options are available, the sound pressure levels SHALL be provided for the various fan speed options.

OBSERVATION: A-weighted sound power level, $L_{WA,}$, may also be provided. This acoustic testing SHOULD be carried out according to ISO-7779 on a standard test table.

3.13 PXI Express Compatibility Glyphs

3.13.1 Module Glyphs

RULE: The PXI Express System Module compatibility glyph shown in Figure 3-13 SHALL be visible on front panels of PXI Express System Modules.

RULE: The PXI Express Peripheral Module compatibility glyph shown in Figure 3-13 SHALL be visible on front panels of PXI Express Peripheral Modules.

RULE: The PXI Express System Timing Module compatibility glyph shown in Figure 3-13 SHALL be visible on front panels of PXI Express System Timing Modules.

OBSERVATION: PXI-1 Modules and Hybrid Slot Compatible PXI-1 Modules have visible the Peripheral Module glyph defined in the PXI-1 specification.

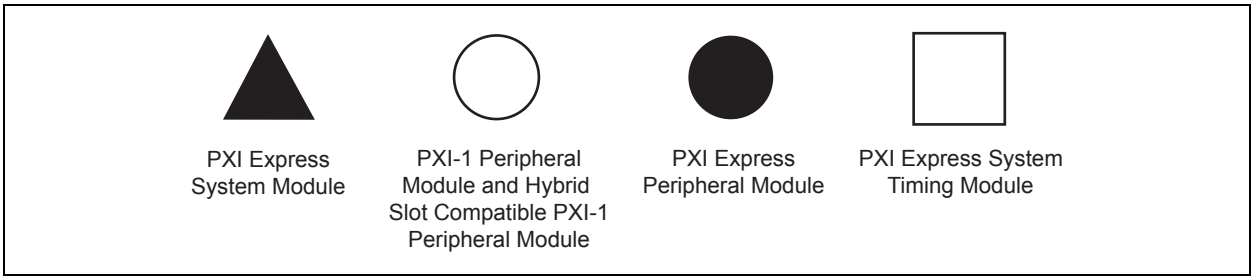

Figure 3-13. Module Glyphs

3.13.2 Chassis Slot Glyphs

RULE: The PXI Express System Slot compatibility glyph shown in Figure 3-14 SHALL be visible directly below the PXI Express System Slot on a PXI Express Chassis with the slot number indicated inside the glyph.

RULE: The PXI Express Peripheral Slot compatibility glyph shown in Figure 3-14 SHALL be visible directly below the PXI Express Peripheral Slots on a PXI Express Chassis with the slot number indicated inside the glyph.

RULE: The PXI Express Hybrid Slot compatibility glyph shown in Figure 3-14 SHALL be visible directly below the PXI Express Hybrid Slots on a PXI Express Chassis with the slot number indicated inside the glyph.

RULE: The PXI Express System Timing Slot compatibility glyph shown in Figure 3-14 SHALL be visible directly below the PXI Express System Timing Slot on a PXI Express Chassis with the slot number indicated inside the glyph.

OBSERVATION: PXI-1 Slots have visible the Peripheral Slot glyph defined in the PXI-1 specification.

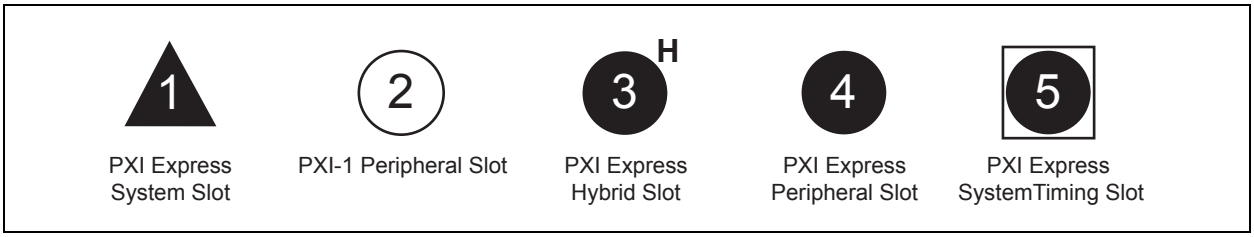

Figure 3-14. Slot Glyphs

4. Electrical Requirements

This section discusses the detailed electrical requirements for developing PXI Express-compatible Peripheral Modules, System Modules, System Timing Modules, and backplanes. It also discusses appropriate connector pinouts, power supply requirements, and 6U form factor implementation issues.

4.1 PCI Signals

PXI Express backplanes may contain Hybrid Slots or PXI-1 Slots. These slots contain pins for PCI functionality that are defined in the PXI-1 and PICMG 2.0 specifications.

4.1.1 Hybrid Slot Requirements

RULE: Hybrid Slots in PXI Express backplanes SHALL meet the requirements of the PXI-1 specification for the signals on the P1 connector.

RULE: The address line to IDSEL mapping based on logical slot number defined in the PICMG 2.0 specification SHALL be used for Hybrid Slots.

RULE: The interrupt assignments based on logical slot number defined in the PICMG 2.0 specification SHALL be used for Hybrid Slots.

4.1.2 PXI-1 Slot Requirements

RULE: PXI-1 slots in PXI Express backplanes SHALL meet the requirements of the PXI-1 specification for the signals on the P1 and P2 connectors.

RULE: The address line to IDSEL mapping based on logical slot number defined in the PICMG 2.0 specification SHALL be used for PXI-1 slots.

RULE: The interrupt assignments based on logical slot number defined in the PICMG 2.0 specification SHALL be used for PXI-1 slots.

4.2 CPCI Express Signals

The signals involved in PCI Express communication, as well as various sideband signals used by PXI Express Modules and slots, are defined in the *CompactPCI Express Specification*. PXI Express developers need to follow the requirements of the *CompactPCI Express Specification* as well as the requirements of this specification when developing PXI Express backplanes and Modules.

4.2.1 System Module/Slot Requirements

RULE: PXI Express System Modules and System Slots SHALL meet all requirements for System Boards and System Slots defined in the *CompactPCI Express Specification* for the signals listed in Table 4-1.

Table 4-1. System Module and Slot Requirements

Signal Name	Note
yPETpx	where y is the Link and x is Lane within a Link
yPETnx	where y is the Link and x is Lane within a Link
yPERpx	where y is the Link and x is Lane within a Link
yPERnx	where y is the Link and x is Lane within a Link
yRefClk+	where y is the Link

Table 4-1. System Module and Slot Requirements (Continued)

Signal Name	Note
yRefClk-	where y is the Link
PWR_OK	
PS_ON	
LINKCAP	
PWRBTN#	
SMBDAT	
SMBCLK	
PERST#	
GA4..GA0	
SYSEN#	
WAKE#	
ALERT#	
I/O	Several of these signals are defined within this specification for instrumentation functionality.
RSV	Several of these signals are defined within this specification for instrumentation functionality.
12V	
5V	
3.3V	
5VAux	
GND	

Within the *CompactPCI Express Specification*, two backplane routing schemes are allowed for the System Slot: a 4 Link configuration and a 2 Link configuration.

PERMISSION: PXI Express backplanes MAY follow either the 4 Link routing configuration or the 2 Link routing configuration as defined by the *CompactPCI Express Specification*.

RULE: System Modules SHALL provide 4 Links.

PERMISSION: Some System Modules MAY be able to combine the four smaller Links into two larger Links.

4.2.2 PXI Express Peripheral Module / Slot Requirements

RULE: PXI Express Peripheral Modules and Peripheral Slots SHALL meet all requirements for Type 2 Peripheral Boards and Type 2 Peripheral Slots defined in the *CompactPCI Express Specification* for the signals listed in Table 4-2.

Table 4-2. PXI Express Peripheral Module and Slot Requirements

Signal Name	Note
yPETpx	where y is the Link and x is Lane within a Link
yPETnx	where y is the Link and x is Lane within a Link
yPERpx	where y is the Link and x is Lane within a Link
yPERnx	where y is the Link and x is Lane within a Link
yRefClk+	where y is the Link
yRefClk-	where y is the Link
ATNLED	
ATNSW#	
PRSNT#	
PWREN#	
MPWRGD#	
SMBDAT	
SMBCLK	
PERST#	
GA4..GA0	
SYSEN#	
WAKE#	
ALERT#	
I/O	Several of these signals are defined within this specification for instrumentation functionality.
RSV	Several of these signals are defined within this specification for instrumentation functionality.
12V	
3.3V	
5VAux	
GND	

4.2.3 System Timing Module/Slot Requirements

RULE: PXI Express System Timing Modules and System Timing Slots SHALL meet all requirements for Type 2 Peripheral Boards and Type 2 Peripheral Slots defined in the *CompactPCI Express Specification* for the signals listed in Table 4-3.

Table 4-3. System Timing Module and Slot Requirements

Signal Name	Note
yPETpx	where y is the Link and x is Lane within a Link
yPETnx	where y is the Link and x is Lane within a Link
yPERpx	where y is the Link and x is Lane within a Link
yPERnx	where y is the Link and x is Lane within a Link
yRefClk+	where y is the Link
yRefClk-	where y is the Link
ATNLED	
ATNSW#	
PRSNT#	
PWREN#	
MPWRGD#	
SMBDAT	
SMBCLK	
PERST#	
GA4..GA0	
SYSEN#	
WAKE#	
ALERT#	
I/O	Several of these signals are defined within this specification for instrumentation functionality.
RSV	Several of these signals are defined within this specification for instrumentation functionality.
12V	
3.3V	
5VAux	
GND	

4.2.4 Hybrid Slot Requirements

RULE: PXI Express Hybrid Slots SHALL meet all requirements for Type 2 Peripheral Slots defined in the *CompactPCI Express Specification* for the signals listed in Table 4-4.

Table 4-4. Hybrid Slot Requirements

Signal Name	Note
yPETpx	where y is the Link and x is Lane within a Link
yPETnx	where y is the Link and x is Lane within a Link
yPERpx	where y is the Link and x is Lane within a Link
yPERnx	where y is the Link and x is Lane within a Link
yRefClk+	where y is the Link
yRefClk-	where y is the Link
ATNLED	
ATNSW#	
PRSNT#	
PWREN#	
MPWRGD#	
SMBDAT	
SMBCLK	
PERST#	
GA4..GA0	
SYSEN#	
WAKE#	
ALERT#	
I/O	Several of these signals are defined within this specification for instrumentation functionality.
RSV	Several of these signals are defined within this specification for instrumentation functionality.
12V	
5V	
3.3V	
5VAux	
GND	

4.3 PXI-1 Instrumentation Signals

This specification retains all the timing and synchronization capabilities of the PXI-1 specification. That feature set can solve a wide range of system applications and remains a key advantage for PXI systems. Retaining this complete compatibility also allows for seamless migration of existing architectures into new PXI Express systems.

4.3.1 Reference Clock: PXI_CLK10

The PXI_CLK10 signal remains a primary method of synchronization of PXI Modules and is carried forward to this specification. Due to the relationship between PXI_CLK10 and PXIe_CLK100, the rules for implementing PXI_CLK10 within PXI Express backplanes, Peripheral Modules, and System Timing Modules is defined in the *PXI Express Timing References* section of this specification. The requirements in this section for PXI_CLK10 make it compatible with PXI-1 Peripheral Modules.

4.3.2 Trigger Bus

RULE: The trigger bus, PXI_TRIG[0:7], on PXI Express Chassis, Peripheral Modules, System Modules, and System Timing Modules SHALL meet the electrical requirements in PXI-1 for all rules, except the following changes.

(1) The definition of a PXI segment no longer depends on a PCI bridging segments. It is inconvenient and adds no value to tie Data Bus topology and Trigger Bus topology.

RULE: For each PXI trigger bus segment in a PXI Chassis, the PXI Chassis SHALL bus the PXI_TRIG[0:7] signal to each PXI slot (System and Peripheral) in that segment. A Chassis SHALL NOT directly connect PXI_TRIG buses from different PXI trigger bus segments. If a System Slot controls multiple PXI segments, it SHALL NOT directly connect PXI trigger buses from different segments. A trigger bus segment SHALL NOT have more than eight trigger loads. A trigger load is defined as a trigger buffer device or Slot connection.

(2) Termination is added to both ends of the trigger bus to improve signal quality by more effectively preventing reflections.

RULE: PXI_TRIG[0:7] SHALL be AC terminated with a 50 Ω resistor and 33 pf cap at both ends of the bus segment in addition to the diode termination required in the PXI-1 specification as shown in Figure 4-1.

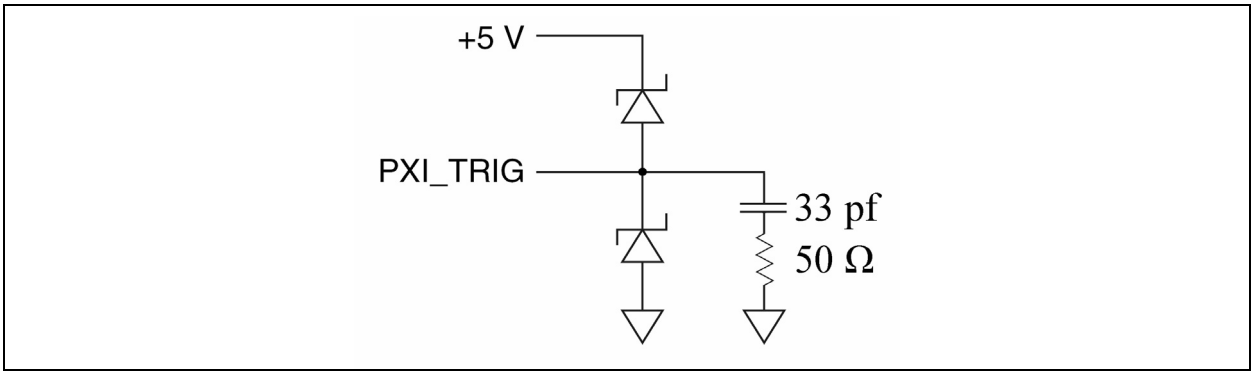

Figure 4-1. PXI Trigger Bus Termination

(3) A pullup is added to the backplane to guarantee a stable state on the trigger line when the bus is in high impedance. The Module pull-up restriction is simplified.

RULE: PXI_TRIG[0:7] SHALL be pulled to the 5 V rail with a 2.2 KΩ pullup on one end of the bus segment.

PERMISSION: Modules MAY place a pull-up of 20 KΩ or greater value on PXI_TRIG[0:7].

(4) The characteristic impedance of the backplane is changed to 65 Ω ± 10% to allow backplanes to be built with more cost-effective trace widths.

RULE: The *unloaded* characteristic impedance for the backplane $Z_{l,min}$ SHALL be 65 Ω ± 10% using a stripline transmission line geometry.

(5) The maximum length stub allowed on a Module is increased to 3 in. to make Module trigger routing easier.

RULE: Printed circuit board trace lengths for PXI trigger bus signals on modules SHALL be less than or equal to 3 in.

The following new recommendations are made:

RECOMMENDATION: Synchronous trigger Clk to Out–Tval defined in the PXI-1 specification SHOULD be less than 20 ns to allow extra time for the signal to propagate through multiple bus segments and bridges. This recommendation precludes sending data on falling edge and receiving on rising edge.

RECOMMENDATION: Type A drivers are no longer recommended. When sending clocks or edges across the backplane, the driver SHOULD be a slow slew rate driver to minimize reflections.

4.3.3 Star Trigger

The PXI_STAR signal is routed by the backplane as a point-to-point connection back to the System Timing Slot. A System Timing Module may be used in this Slot to have private transmission of clocks of triggers to each Module connected to a PXI_STAR.

RULE: The PXI_STAR signals SHALL meet all requirements called out in the PXI-1 specification.

In the PXI-1 specification, there is a recommended mapping of PXI star triggers to Peripheral Slots. In the case of a PXI Express System Timing Slot, the PXI star triggers are allowed to route to any Peripheral Slot. Software is made aware of this mapping by a `.ini` file.

PERMISSION: A PXI_STAR signal from a PXI Express System Timing Slot MAY route to any slot.

RULE: Every slot in a PXI Express Chassis, except for the PXI Express System Timing Slot, SHALL have a PXI star trigger routed to it from the PXI Express System Timing Slot, unless the number of slots requiring PXI star triggers exceeds the number of available PXI star triggers.

OBSERVATION: The PXI Express System Controller Slot has a PXI star trigger connected to it from the PXI Express System Timing Slot.

OBSERVATION: The PXI_STAR signal to slot mapping is specified in the Chassis `.ini` file according to the format specified in the *PXI Express Software Specification*.

4.3.4 Local Bus

PXI-1 Implemented a 13 line daisy-chained local bus between adjacent Peripheral Slots. PXI Express modules maintain the PXI_LBL6 and PXI_LBR6 signals.

RULE: The PXI_LBL6 and PXI_LBR6 signals SHALL meet all requirements called out in the PXI-1 specification for local bus signals.

OBSERVATION: The PXI Express System Slot has the PXI_LBR6 signal defined but no PXI_LBL6 signal defined because there are no PXI Express Slots to the left of the System Slot.

4.4 PXI Express Timing References

4.4.1 Backplane Requirements

The PXI Express backplane is responsible for providing a common reference clock for synchronization of multiple Modules in an instrumentation system. To that end, the backplane provides 10 MHz and 100 MHz clocks independently to each Peripheral Slot with single-source, single-destination connections. The low slot-to-slot skew makes these clocks ideal for qualifying trigger protocols. The 100 MHz clock is a fast-switching LVPECL clock for precise timing. The 10 MHz TTL/CMOS clock preserves compatibility with PXI Modules.

4.4.1.1 PXIe_CLK100

RULE: The PXIe_CLK100 signal provided by the backplane SHALL be a 100 MHz, differential, 3.3 V LVPECL clock. Its frequency accuracy SHALL be ±100 ppm or better over the specified operating temperature and time.

RULE: When each line of the PXIe_CLK100 pair is terminated with a 50 Ω load to 1.30 V (or Thévenin equivalent), the absolute value of the differential voltage across the pair at the Peripheral Module connector SHALL be 800 mV nominally and SHALL NOT be less than 400 mV (except during transition) or greater than 1000 mV. The V_{OH} level for each line SHALL be greater than 2.0 V and less than 2.5 V.

RULE: The PXIe_CLK100 signal SHALL have a duty cycle between 45% and 55%, measured by the differential 0 V transition times. The 20%-to-80% rise and fall times SHALL NOT exceed 350 ps.

RULE: The PXIe_CLK100 signal to each Peripheral Slot SHALL be driven by an independent differential LVPECL driver. The backplane SHALL transmit the signal to each slot with a balanced transmission line pair having a differential impedance of 100 Ω ± 10 Ω. The backplane SHALL NOT include any termination or bias network on the transmission line.

OBSERVATION: Equivalently, each trace in the transmission line pairs must have an odd-mode impedance of 50 Ω ± 5 Ω.

RULE: The time skew between rising or falling edges of the PXIe_CLK100 signals at any two Peripheral Module connectors SHALL NOT exceed 200 ps. The edges are defined as the differential 0 V transition times and are measured where each signal pin enters the Peripheral Module circuit board.

RECOMMENDATION: PXIe_CLK100 is capable of high performance. Jitter SHOULD be kept under 5 ps rms from 12 kHz to 20 MHz, and 5 ps rms from 10 Hz to 12 kHz.

4.4.1.2 PXI_CLK10

RULE: The PXI_CLK10 provided by the backplane SHALL be a 10 MHz TTL signal, with V_{OH} no less than 2.4 V and V_{OL} no greater than 0.5 V. PXI_CLK10 SHALL NOT exceed 3.3 V.

RULE: The frequency accuracy SHALL be ±100 ppm or better over the specified operating temperature and time.

RULE: The PXI_CLK10 signal SHALL have a duty cycle between 45% and 55%, measured by the 1.5 V transition times.

RULE: The PXI_CLK10 signal to each Peripheral Slot SHALL be driven by an independent buffer that has a source impedance matched to the transmission line. Each transmission line SHALL have 65 Ω ± 10 Ω characteristic impedance, and each driver SHALL have a source impedance of 65 Ω ± 10 Ω.

OBSERVATION: In most cases it will necessary to place a resistor in series with the driver so that the total output impedance is 65 Ω.

RULE: The time skew between the rising or falling edges of the PXI_CLK10 signals at any two Peripheral Module connectors SHALL NOT exceed 1 ns. The edges are defined as the 1.5 V transition times and are measured where each signal pin enters the Peripheral Module circuit board.

RECOMMENDATION: The use of low-cost PLL buffers for driving the clock to each slot MAY lead to excessive jitter and therefore SHOULD NOT be used.

4.4.1.3 PXIe_SYNC100

PXIe_SYNC100 is a differential signal distributed to each Peripheral Slot by the Chassis backplane resource. PXIe_SYNC100 asserts as a 10 ns pulse synchronous to PXIe_CLK100 with a frequency determined by the system. The assertion of that pulse is coordinated with the rising edge of the PXI_CLK10 signal.

The relationship of PXIe_SYNC100 to PXI_CLK10 allows a Peripheral Module to create a local version of PXI_CLK10 that is in phase with the PXI_CLK10 signal and can be used to send triggers to, and receive triggers from, devices that use PXI_CLK10. A device receiving PXIe_SYNC100 in this manner can therefore perform PXI_CLK10-synchronous communication without actually connecting to the PXI_CLK10 signal. This can be useful for devices with PLLs or DLLs that cannot lock to a frequency as low as 10 MHz.

RULE: The PXIe_SYNC100 signal provided by the backplane SHALL be a differential 3.3 V LVPECL signal.

RULE: When each line of the PXIe_SYNC100 pair is terminated with a 50 Ω load to 1.30 V (or Thévenin equivalent), the absolute value of the differential voltage across the pair at the Peripheral Module connector SHALL be 800 mV nominally and SHALL NOT be less than 400 mV (except during transition) or greater than 1000 mV. The V_{OH} level for each line SHALL be greater than 2.0 V and less than 2.5 V.

RULE: The 20%-to-80% rise and fall times for PXIe_SYNC100 SHALL NOT exceed 350 ps.

RULE: The PXIe_SYNC100 signal to each Peripheral Slot SHALL be driven by an independent differential LVPECL driver. The backplane SHALL transmit the signal to each slot with a balanced transmission line pair having a differential impedance of 100 Ω ± 10 Ω. The backplane SHALL NOT include any termination or bias network on the transmission line.

OBSERVATION: Equivalently, each trace in the transmission line pairs must have an odd-mode impedance of 50 Ω ± 5 Ω.

4.4.1.4 Timing, Switching, and PXIe_SYNC_CTRL

RULE: PXI_CLK10 SHALL be synchronous to PXIe_CLK100. Each rising edge of PXI_CLK10 SHALL assert no earlier than 1 ns before the rising edge of PXIe_CLK100 and no later than 6.5 ns after the PXIe_CLK100 rising edge, as measured where each signal pin enters the Peripheral Module circuit board. The rising edges are defined as the differential 0 V transition times for PXIe_CLK100 and 1.5 V transition times for PXI_CLK10.

Figure 4-2 and Table 4-5 illustrate this relationship:

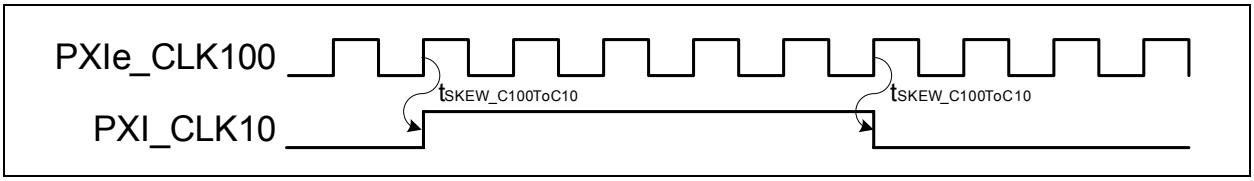

Figure 4-2. Timing relationship of PXI_CLK10 to PXIe_CLK100

Table 4-5. Timing relationship of PXI_CLK10 to PXIe_CLK100

Description	Parameter	Min	Max
Delay from rising edge of PXIe_CLK100 to either edge of PXI_CLK10 (at PXI Express connector)	$t_{SKEW\_C100ToC10}$	-1 ns	6.5 ns

RECOMMENDATION: A backplane SHOULD allow PXI_CLK10 and PXIe_CLK100 to be derived from the PXI_CLK10_IN signal from the System Timing Slot or another external source to allow for a more accurate or stable reference.

RULE: If a backplane allows PXI_CLK10 to be received from the System Timing Slot, the backplane SHALL have a 1500 Ω ± 5% pull-down resistor to ground on the PXIe_CLK10_IN signal. The receiving circuitry for this signal on the backplane SHALL be TTL compatible and 5V tolerant, with V_{IH} no greater than 2.0 V and V_{IL} no less than 0.8 V.

RULE: If PXI_CLK10 is switched between sources, the minimum pulse width (high or low) created on PXI_CLK10 SHALL NOT be less than 30 ns and the minimum time between successive edges of the same polarity SHALL NOT be less than 80 ns. The minimum pulse width (high or low) created on PXIe_CLK100 SHALL NOT be less than 2.5 ns and the minimum time between successive edges of the same polarity SHALL NOT be less than 8 ns.

OBSERVATION: The preceding rule is intended to prevent a state machine from being corrupted by glitches in the clock during transition.

RULE: The PXI Express backplane resource SHALL ensure that PXI_CLK10 asserts with the next rising edge of PXIe_CLK100 after the rising edge of PXIe_CLK100 where PXIe_SYNC100 was asserted.

RULE: PXIe_SYNC100 SHALL meet the timing requirements shown in Figure 4-3 and Table 4-6, as measured where each signal pin enters the Peripheral Module circuit board.

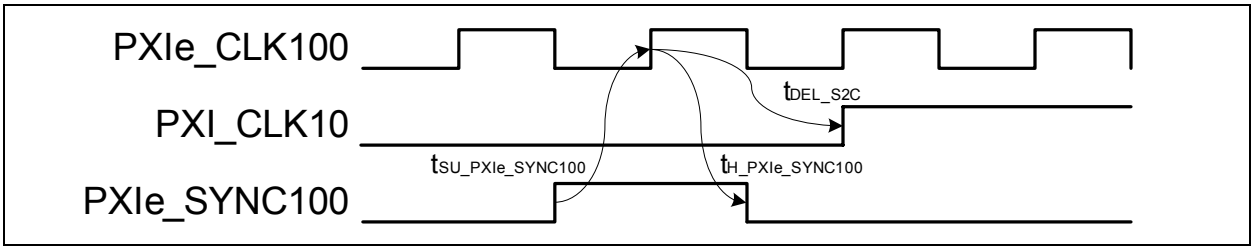

Figure 4-3. Timing Relationship of PXIe_SYNC100 to PXI_CLK10 and PXIe_CLK100

Table 4-6. Timing Relationship of PXIe_SYNC100 to PXI_CLK10 and PXIe_CLK100

Description	Parameter	Min	Max
Setup from edge of PXIe_SYNC100 to rising edge of PXIe_CLK100 (at PXIe connector)	$t_{SU\_PXIe\_SYNC100}$	3 ns	—
Hold from rising edge of PXIe_CLK100 to edge of PXIe_SYNC100 (at PXIe connector)	$t_{H\_PXIe\_SYNC100}$	1 ns	—
Delay from rising edge of PXIe_CLK100 where PXIe_SYNC100 is asserted to next rising edge of PXI_CLK10 (at PXIe connector)	t_{DEL_S2C}	10 ns + $t_{SKEW\_C100ToC10.min}$	10 ns + $t_{SKEW\_C100ToC10.max}$

OBSERVATION: Timing parameter t_{DEL_S2C} is listed to illustrate the relationship between PXIe_SYNC100 and PXI_CLK10 and will be met automatically if all other timing rules are followed.

Figure 4-4 shows an expanded relationship of PXIe_CLK100, PXIe_SYNC100, and PXI_CLK10. In this example, PXIe_SYNC100 has the default 10 MHz behavior.

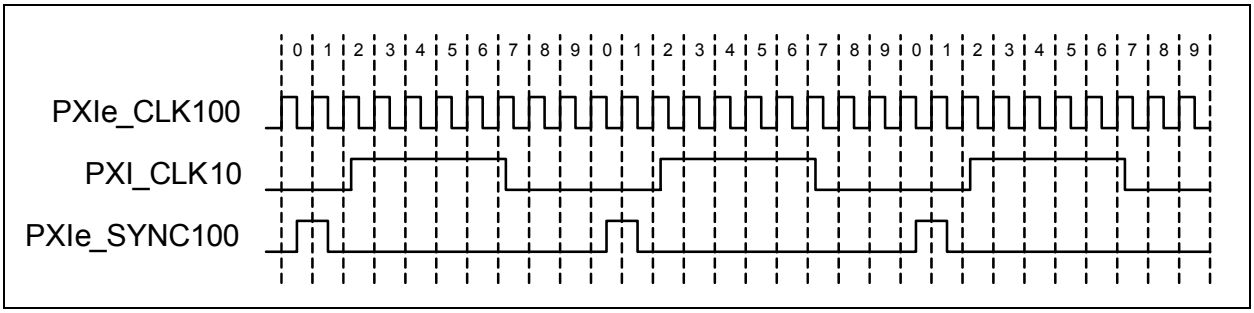

Figure 4-4. PXIe_SYNC100 Default Behavior

In Figure 4-4, PXIe_SYNC100 pulses high for one PXIe_CLK100 cycle and remains low for 9 PXIe_CLK100 cycles. The high pulse precedes the rising edge of PXIe_CLK10, making the creation of an onboard version of PXI_CLK10 possible. Refer to the PXI Express Peripheral Module Requirements section for more information.

RULE: The PXI Express backplane resource SHALL implement the PXIe_SYNC100 default behavior.

PERMISSION: PXIe_SYNC100 MAY be driven by the backplane at a frequency other than 10 MHz, including driving it as a nonperiodic signal, as long as its assertion and deassertion follow the timing rules in the above table.

PERMISSION: When a backplane implements nondefault behavior for PXIe_SYNC100, the backplane MAY use PXIe_SYNC_CTRL from the System Timing Module to control that behavior.

The above permissions allow devices to use PXIe_SYNC100 to communicate via synchronous triggers even when those devices are electrically farther apart than 100 ns. For example, two PXIe Chassis can coordinate their PXIe_SYNC_CTRL signals so that their PXIe_SYNC100 signals toggle at 5 MHz in phase with each other. Instead of using CLK10 to send and receive triggers, Modules in each Chassis use flip-flops clocked by PXIe_CLK100 and enabled by PXIe_SYNC100. With a 5 MHz PXIe_SYNC100, these Modules now have 200 ns to propagate a trigger from a device in one Chassis to a device in another. And because

PXIe_SYNC100 always maintains its relationship to PXIe_CLK10, the performance of Modules that use PXI_CLK10 is not affected.

The System Timing Module drives PXIe_SYNC_CTRL synchronous to PXI_CLK10 and is used by the backplane resource to determine when to assert PXIe_SYNC100. Figures 4-5 and 4-6 show some possible behaviors:

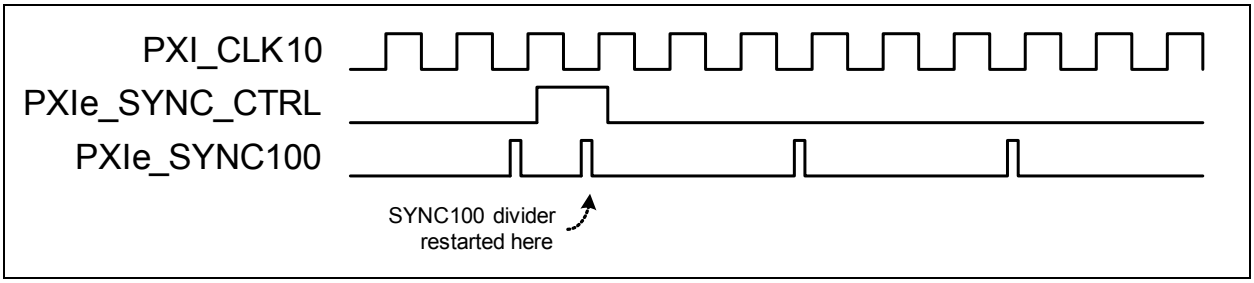

Figure 4-5. PXIe_SYNC100 at 3.33 MHz Using PXIe_SYNC_CTRL as Restart

In this case, the backplane resource is configured to drive PXIe_SYNC100 at 3.33 MHz and to use PXIe_SYNC_CTRL to reset its counter. The assertion of PXIe_SYNC_CTRL causes the counter to start over, adjusting the phase of the PXIe_SYNC100 signal. This allows multiple Chassis that create 3.33 MHz PXIe_SYNC100 signals to have their respective PXIe_SYNC100 signals in phase with each other.

RULE: If a backplane receives PXIe_SYNC_CTRL from the System Timing Slot, the PXI Express backplane resource default behavior SHALL be to interpret a high level on PXIe_SYNC_CTRL as a synchronous restart, according to Figure 4-5. The PXI Express backplane resource default behavior SHALL ignore a low level on PXIe_SYNC_CTRL.

RULE: A PXI Express backplane resource that implements behaviors for PXIe_SYNC_CTRL other than the default behavior SHALL implement the default behavior until programmed to do otherwise at run time.

Figure 4-6 shows an alternate behavior for PXIe_SYNC_CTRL.

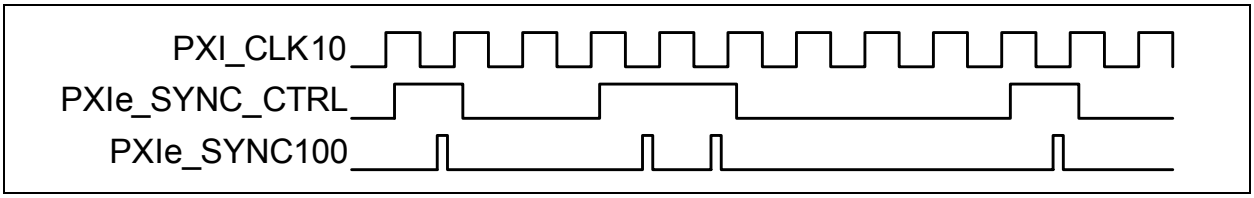

Figure 4-6. PXIe_SYNC100 Using PXIe_SYNC_CTRL as Enable

In this case, the backplane resource uses PXIe_SYNC_CTRL as an enable. Every rising PXI_CLK10 edge where PXIe_SYNC_CTRL is Asserted is preceded by a PXIe_SYNC100 pulse.

RULE: If a backplane receives PXIe_SYNC_CTRL from the System Timing Slot, the backplane SHALL have a pull-down resistor to ground on the PXIe_SYNC_CTRL signal with a value between 10 KΩ and 100 KΩ. Receiving circuitry for this signal on the backplane SHALL have a minimum VIH no greater than 2.0 V and a maximum VIL no less than 0.8 V.

4.4.2 System Timing Module Requirements

RULE: If a System Timing Module drives the SYNC_CTRL signal, it SHALL ensure SYNC_CTRL meets the timing requirements shown in Figure 4-7 and Table 4-7.

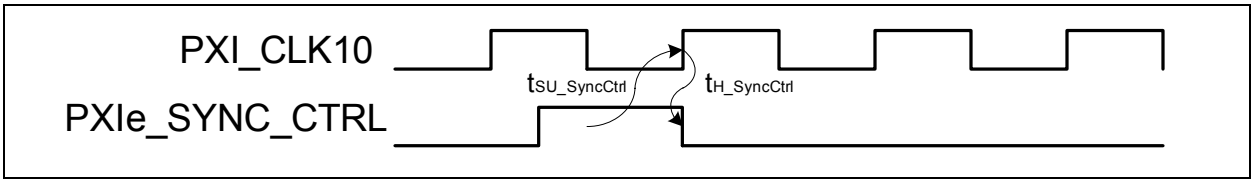

Figure 4-7. Timing Relationship between SYNC_CTRL and PXI_CLK10

Table 4-7. Timing Relationship between SYNC_CTRL and PXI_CLK10

Description	Parameter	Min	Max
Setup from edge of PXIe_SYNC_CTRL to rising edge of PXI_CLK10 (at PXI Express connector)	$t_{SU\_SYNC\_CTRL}$	50 ns	—
Hold from rising edge of PXI_CLK10 to edge of PXIe_SYNC_CTRL (at PXI Express connector)	$t_{H\_SYNC\_CTRL}$	0 ns	—

OBSERVATION: The large minimum time for $t_{SU\_SYNC\_CTRL}$ allows the backplane resource to receive SYNC_CTRL using flip-flops clocked by PXIe_CLK100 and have time to assert PXIe_SYNC100 before the next edge of PXI_CLK10.

RULE: A System Timing Module driving PXI_CLK10_IN SHALL have a driver with a source impedance of 65 Ω ± 10%. The characteristic impedance of the circuit board trace from the driver to the PXI_CLK10_IN connection SHALL be 65 Ω ± 10%. The signal SHALL be a 10 MHz TTL signal, with VOH no less than 2.4 V and VOL no greater than 0.5 V.

OBSERVATION: In most cases it will necessary to place a resistor in series with the driver so that the total output impedance is 65 Ω.

4.4.3 Peripheral Module Requirements

4.4.3.1 PXIe_CLK100

RULE: If a Peripheral Module uses PXIe_CLK100, it SHALL terminate both lines with a 50 Ω (±5 Ω) load to 1.3 V (±0.2 V) or Thévenin equivalent. If a Peripheral Module does not use PXIe_CLK100, it SHALL leave the lines unconnected and unterminated.

RECOMMENDATION: Peripheral Modules SHOULD terminate the PXIe_CLK100 signal with the following circuit:

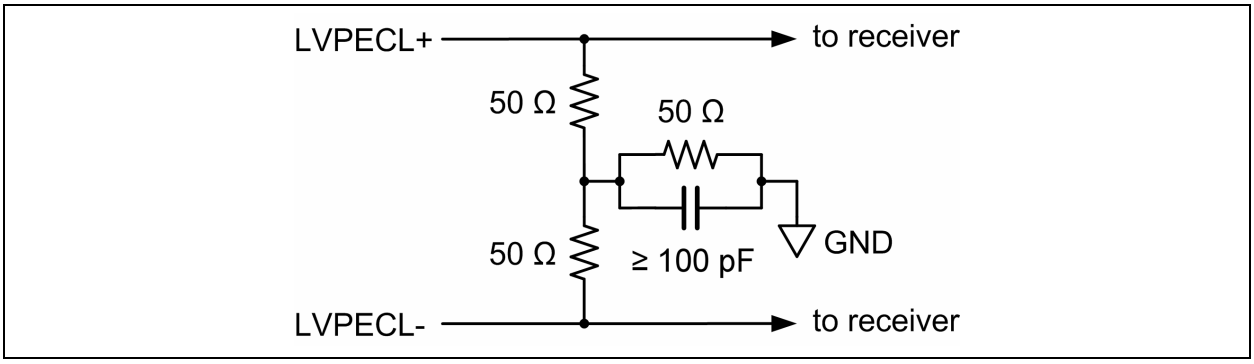

Figure 4-8. Peripheral Module Circuit for Terminating PXIe_CLK100 Signal

RULE: Peripheral Modules SHALL NOT terminate PXIe_CLK100 more than 1 ns of electrical length beyond the backplane connector. Any transmission line between the backplane connector and the termination SHALL have a characteristic differential impedance of 100 Ω ± 10 Ω.

RECOMMENDATION: Because of the fast rise- and fall-times of the PXIe_CLK100 signal, signal integrity will be best at or very near the termination. In Peripheral Modules, the electrical length of the connections beyond the termination SHOULD NOT exceed 160 ps, which in typical glass-epoxy circuit boards is about 25 mm trace length. To maintain good signal integrity, Peripheral Modules SHOULD connect only one active receiver to PXIe_CLK100. If more than one receiver is used, the configuration SHOULD be simulated carefully to ensure that the waveforms are well behaved.

4.4.3.2 PXI_CLK10

RULE: Peripheral Module PXI_CLK10 Receivers SHALL be 3.3 V tolerant, with V_{IH} no greater than 2.0 V and V_{IL} no less than 0.8 V. Peripheral Modules SHALL NOT terminate PXI_CLK10. Board traces from the connector to the PXI_CLK10 Receivers SHALL have a characteristic impedance of 65 Ω ± 10 Ω.

4.4.3.3 PXIe_SYNC100

RULE: If a Peripheral Module uses PXIe_SYNC100, it SHALL terminate both lines with a 50 Ω (±5 Ω) load to 1.3 V (±0.2 V) or Thévenin equivalent. If a Peripheral Module does not use PXIe_SYNC100, it SHALL leave the lines unconnected and unterminated.

RECOMMENDATION: Peripheral Modules SHOULD terminate the PXIe_SYNC100 signal with the following circuit:

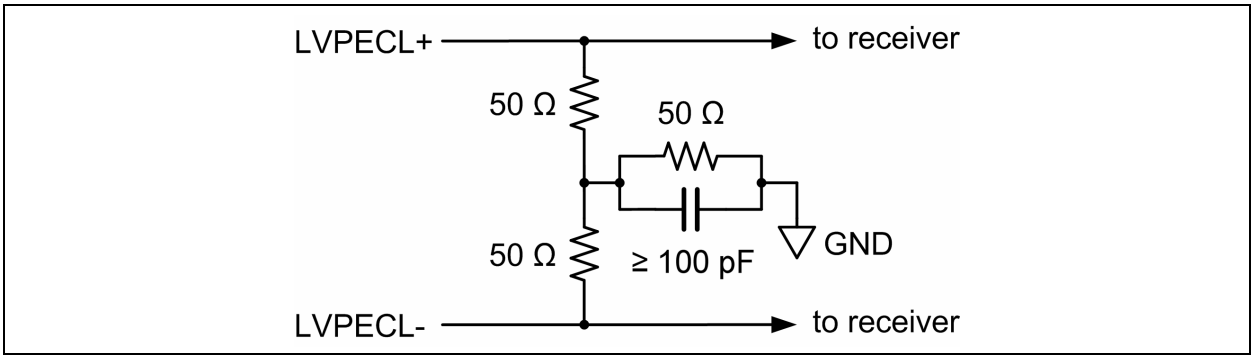

Figure 4-9. Peripheral Module Circuit for Terminating PXIe_SYNC100 Circuit

RULE: Peripheral Modules SHALL NOT terminate PXIe_SYNC100 more than 1 ns of electrical length beyond the backplane connector. Any transmission line between the backplane connector and the termination SHALL have a characteristic differential impedance of 100 Ω ± 10 Ω.

RECOMMENDATION: Because of the fast rise and fall-times of the PXIe_SYNC100 signal, signal integrity will be best at or very near the termination. In Peripheral Modules, the electrical length of the connections beyond the termination SHOULD NOT exceed 160 ps, which in typical glass-epoxy circuit boards is about 25 mm trace length. To maintain good signal integrity, Peripheral Modules SHOULD connect only one active receiver to PXIe_CLK100. If more than one receiver is used, the configuration SHOULD be simulated carefully to ensure that the waveforms are well behaved.

Because the assertion of PXIe_SYNC100 always precedes the rising edge of PXI_CLK10 according to the rules above, a PXI Express Peripheral Module can create a signal that is in phase with PXI_CLK10 without connecting to PXIe_CLK10.

Figure 4-10 shows an example of a circuit that accomplishes this.

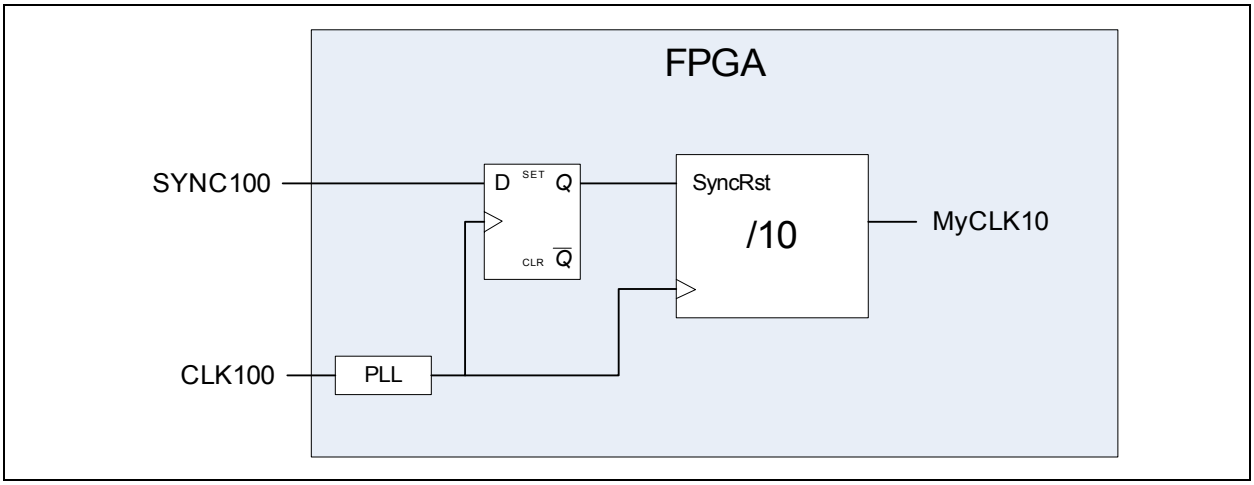

Figure 4-10. Circuit to recreate PXI_CLK10 Internally as MyCLK10

SYNC100 is captured by a flip-flop, the output of which is used to synchronously reset a divider that divides PXIe_CLK100 by 10. The resulting signal is in phase with PXI_CLK10. Note that this circuit will create a signal in phase with PXI_CLK10 even if the frequency of PXIe_SYNC100 is not 10 MHz.

OBSERVATION: The maximum skew of MyCLK10 and PXI_CLK10 is determined by the skew of PXIe_CLK100 between slots, the skew between PXI_CLK10 and PXIe_CLK100, the clock-to-out time of flip-flops internal to the FPGA, and the insertion delay of the PXIe_CLK100 signal (including added jitter).

4.5 Differential Triggers

The PXIe_DSTARA, PXIe_DSTARB, and PXIe_DSTARC signals are differential point-to-point connections between the System Timing Slot and the Peripheral Slots. For each of these three signals, there is an independent differential pair between each Peripheral Slot and the System Timing Slot. Additionally, all signals are matched length.

PXIe_DSTARA is designed for distributing high-speed, high-quality clock signals from the System Timing Slot to the peripherals.

PXIe_DSTARB is designed for distributing high-speed, high-quality trigger signals from the System Timing Slot to the peripherals.

PXIe_DSTARC is designed for sending high-speed, high-quality trigger or clock signals from the peripherals to the System Timing Slot.

The PXIe_DSTARA signal is a fast-switching LVPECL clock for precise timing. The PXIe_DSTARB and PXIe_DSTARC signals are fast-switching LVDS clock/triggers for high-speed synchronization while maintaining compatibility with common FPGAs and other ICs.

4.5.1 Chassis Requirements

If a PXI Express System Timing Slot is implemented within a PXI Express Chassis, there will be a set of three differential pairs connecting each slot to the System Timing Slot in a star configuration for the purpose of timing and synchronization. The low slot-to-slot skew and signal-to-signal skew make these ideal for transferring a clock and synchronous trigger. These differential pairs will be referred to as a PXIe DSTAR set. To make backplane routing possible and reasonable, the Chassis developer will have the flexibility to route any PXIe DSTAR set to any slot provided that members of the set are not split between separate slots.

The rules and recommendations in this section only apply if the PXI Express Chassis implements a System Timing Slot.

RULE: A PXIe DSTAR set SHALL be defined as containing the three differential signal pairs (PXIe_DSTARA***n***, PXIe_DSTARB***n***, PXIe_DSTARC***n***), where ***n*** denotes the PXIe DSTAR set number.

RULE: All differential pairs within a PXIe DSTAR set SHALL be routed to the same slot.

RULE: If a PXIe DSTAR set is routed to a Peripheral Slot, its signals SHALL be connected to the Peripheral Slot according to Table 4-8, where ***n*** denotes PXIe DSTAR set number.

Table 4-8. PXIe_DSTAR Set Mapping

Differential System Timing Pair	Peripheral Slot Pair on XP3
PXIe_DSTARA***n***+	PXIe_DSTARA+
PXIe_DSTARA***n***-	PXIe_DSTARA-
PXIe_DSTARB***n***+	PXIe_DSTARB+
PXIe_DSTARB***n***-	PXIe_DSTARB-

Table 4-8. PXIe_DSTAR Set Mapping (Continued)

Differential System Timing Pair	Peripheral Slot Pair on XP3
PXIe_DSTARC***n***+	PXIe_DSTARC+
PXIe_DSTARC***n***-	PXIe_DSTARC-

PERMISSION: A PXIe DSTAR set MAY be routed to the PXIe_DSTARA, PXIe_DSTARB and PXIe_DSTARC pins on any slot.

RULE: If a slot is connected to a PXIe DSTAR set from the System Timing Slot, it SHALL only be connected to the signals from one PXIe DSTAR set.

RULE: One PXIe DSTAR set SHALL be routed back to the PXI Express System Timing Slot XP3 connector following the interpair and pair-to-pair length matching requirements placed on these signals in this section.

RULE: Every PXI Express Peripheral Slot, PXI Express Hybrid Slot and PXI Express System Timing Slot SHALL have a PXIe DSTAR set routed to it from the PXI Express System Timing Slot unless the total number of these slots exceeds the number of available PXIe DSTAR sets.

OBSERVATION: The PXIe DSTAR set to slot mapping is specified in the Chassis `.ini` file according to the format specified in the *PXI Express Software Specification*.

OBSERVATION: The pinout for the System Timing Slot was chosen so that when placed in the middle of a backplane, the signal lengths can be kept to a minimum and the layer count will be minimized by keeping all or most of the differential pairs on one routing layer.

RULE: The backplane SHALL route the PXIe_DSTAR signals to each slot with balanced transmission line pairs having a differential impedance of 100 Ω ± 10 Ω.

OBSERVATION: Equivalently, each trace in the transmission line pairs SHOULD have an odd-mode impedance of 50 Ω ± 5 Ω.

RECOMMENDATION: All PXIe_DSTARA, PXIe_DSTARB, and PXIe_DSTARC pairs SHOULD be routed on a single layer referenced to a solid ground plane to improve radiated immunity when traces are floating.

RULE: The time skew of the propagation delay of any two PXIe_DSTAR pairs (including all PXIe_DSTARA, PXIe_DSTARB, and PXIe_DSTARC signals) across the backplane SHALL NOT exceed 150 ps, including the backplane connectors.

RULE: The time skew of the propagation delay of the two signals within a PXIe_DSTAR differential pair across the backplane SHALL NOT exceed 25 ps, including the backplane connectors.

4.5.2 PXIe Peripheral Module / Slot Requirements

4.5.2.1 PXIe_DSTARA

RULE: If a Peripheral Module receives PXIe_DSTARA, it SHALL terminate both lines with a 50 Ω (±5 Ω) load to 1.3 V (±0.2 V) or Thévenin equivalent. If a Peripheral Module does not receive PXIe_STARA, it SHALL leave the lines unconnected and unterminated.

RECOMMENDATION: Peripheral Modules that are receiving PXIe_DSTARA SHOULD terminate the PXIe_DSTARA signal with the following circuit:

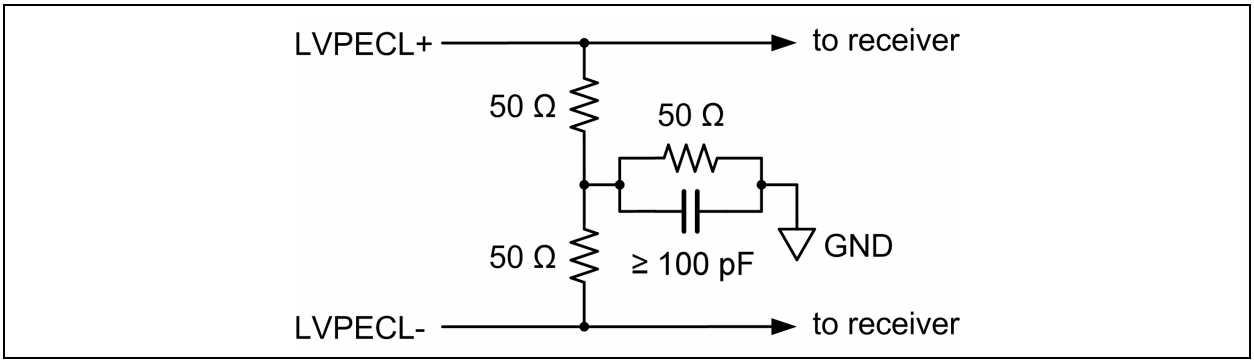

Figure 4-11. Peripheral Module Circuit for Terminating PXIe_DSTARA

RULE: Peripheral Modules SHALL NOT terminate PXIe_DSTARA more than 1 ns of electrical length beyond the backplane connector. Any transmission line between the backplane connector and the termination SHALL have a characteristic differential impedance of 100 Ω ± 10 Ω.

RECOMMENDATION: Because of the fast rise and fall-times of the PXIe_DSTARA signal, signal integrity will be best at or very near the termination. The electrical length of the connections between the termination and the LVPECL Receiver SHOULD NOT exceed 160 ps, which in typical glass-epoxy circuit boards is about 25 mm trace length. To maintain good signal integrity, Peripheral Modules SHOULD connect only one active receiver to PXIe_DSTARA. If more than one receiver is used, the configuration SHOULD be simulated carefully to ensure that the waveforms are well behaved.

4.5.2.2 PXIe_DSTARB

RULE: If a Peripheral Module receives PXIe_DSTARB, it SHALL terminate the lines with a 100 Ω ± 10 Ω differential resistor.

RULE: Peripheral Modules SHALL NOT terminate PXIe_DSTARB more than 1 ns of electrical length beyond the backplane connector. Any transmission line between the backplane connector and the termination SHALL have a characteristic differential impedance of 100 Ω ± 10 Ω.

RECOMMENDATION: Because of the fast rise and fall-times of the PXIe_DSTARB signal, signal integrity will be best at or very near the termination. The electrical length of the connections between the termination and the LVDS Receiver SHOULD NOT exceed 160 ps, which in typical glass-epoxy circuit boards is about 25 mm trace length. To maintain good signal integrity, Peripheral Modules SHOULD connect only one active receiver to PXIe_DSTARB. If more than one receiver is used, the configuration SHOULD be simulated carefully to ensure that the waveforms are well behaved.

4.5.2.3 PXIe_DSTARC

RULE: If the Peripheral Module chooses to implement PXIe_DSTARC, the signal provided SHALL be a differential, LVDS signal. The Peripheral Module SHALL transmit the signal to the System Timing Slot with a balanced transmission line pair having a differential impedance of 100 Ω ± 10 Ω.

RULE: When the PXIe_DSTARC pair is terminated with a 100 Ω differential load at the Receiver, the voltage levels at the connector to the System Timing Module SHALL be compliant with the TIA/EIA-644 LVDS specification.

RULE: The signal source SHALL ensure that the LVDS driver is off (either tri-stated or driving a constant) by default, and MAY only enable it under software control when a Receiver with a 100 Ω differential termination resistor is known to exist.

4.5.3 System Timing Module/Slot Requirements

4.5.3.1 PXIe_DSTARA

RULE: The PXIe_DSTARA signals provided by the System Timing Module SHALL be differential 3.3 V LVPECL signals. The System Timing Module SHALL transmit the signals to all slots with balanced transmission line pairs having a differential impedance of 100 Ω ± 10 Ω. The System Timing Module SHALL NOT include any termination or bias network on the transmission lines, except to ensure that each driver is disabled when unterminated by a Module.

RULE: When each line of the PXIe_DSTARA pair is terminated with a 50 Ω load to 1.30 V (or Thévenin equivalent), the absolute value of the differential voltage across the pair at the Peripheral Module connector SHALL be 800 mV nominally and SHALL NOT be less than 400 mV (except during transition) or greater than 1000 mV. The V_{OH} level for each line SHALL be greater than 2.0 V and less than 2.5 V.

OBSERVATION: While many FPGAs have "LVPECL" output drivers, these drivers are generally not compatible with the aforementioned LVPECL requirement.

RULE: The PXIe_DSTARA signal to each Peripheral Slot SHALL be driven by an independent differential LVPECL driver.

RECOMMENDATION: The PXIe_DSTARA signal SHOULD have a duty cycle between 45% and 55%, measured by the differential 0 V transition times. The 20%-to-80% rise and fall times SHOULD NOT exceed 350 ps.

RECOMMENDATION: The time skew between rising or falling edges of the PXIe_DSTARA signals at any two connections to the backplane SHOULD NOT exceed 200 ps. The edges are defined as the differential 0 V transition times.

RECOMMENDATION: System Timing Modules SHOULD specify the maximum skew between all PXIe_DSTARA signals as provided to the pins of the connectors on the System Timing Module which connect it to the backplane.

4.5.3.2 PXIe_DSTARB

RULE: The PXIe_DSTARB signal provided by System Timing Module SHALL be a differential, LVDS signal. The System Timing Module SHALL transmit the signal to each slot with a balanced transmission line pair having a differential impedance of 100 Ω ± 10 Ω.

RULE: When the PXIe_DSTARB pair is terminated with a 100 Ω differential load at the Receiver the voltage levels at the connector to the Peripheral Module SHALL be compliant with the TIA/EIA-644 LVDS specification.

RULE: The signal source SHALL ensure that the LVDS driver is off (either tri-stated or driving a constant) by default, and may only enable it under software control when a Receiver with a 100 Ω differential termination resistor is known to exist.

RULE: The PXIe_DSTARB signal to each Peripheral Slot SHALL be driven by an independent differential LVDS driver.

RECOMMENDATION: System Timing Modules SHOULD specify the maximum skew between all PXIe_DSTARA and PXIe_DSTARB signals, as provided to the pins of the connectors on the System Timing Module which connect it to the backplane.

4.5.3.3 PXIe_DSTARC

RULE: If the System Timing Module receives PXIe_DSTARC, it SHALL terminate the pairs differentially with 100 Ω ± 10 Ω resistors.

RULE: The System Timing Module SHALL NOT terminate PXIe_DSTARC more than 1 ns of electrical length beyond the backplane connector. Any transmission line between the backplane connector and the termination SHALL have a characteristic differential impedance of 100 Ω ± 10 Ω.

RECOMMENDATION: Because of the fast rise and fall-times of the PXIe_DSTARC signal, signal integrity will be best at or very near the termination. The electrical length of the connections between the termination and the LVDS Receivers SHOULD NOT exceed 160 ps, which in typical glass-epoxy circuit boards is about 25 mm trace length. To maintain good signal integrity, the System Timing Module SHOULD connect only one active receiver to each PXIe_DSTARC pair. If more than one receiver is used, the configuration SHOULD be simulated carefully to ensure that the waveforms are well behaved.

4.6 Slot Identification

Slot Identification in PXI Express is performed using the geographical address pins (GA) in each slot. The software mechanisms for reporting the value encoded on these pins is defined in the *PXI Express Software Specification*.

RULE: A PXI Express Module, other than a PXI Express System Module, must provide a software mechanism for the PXI Express System Module to read the value on pins GA(4:0) in the slot where the Module is located.

OBSERVATION: The System Module does not need to report its slot number via software, because it can be assumed to be in Slot 1.

OBSERVATION: PXI-1 Peripheral Modules and Hybrid Slot Compatible PXI-1 Peripheral Modules are not required to provide a software mechanism for the PXI Express System Module to read the value on pins GA(4:0) in the slot where the Module is located.

RULE: A PXI Express Module SHALL include software that reports its slot number using the interfaces specified in the *PXI Express Software Specification*.

4.7 Backplane Identification

RULE: PXI Express Chassis SHALL have the Backplane Identification and Capability Record implemented as a serial EPROM or similar functioning device as defined by the *CompactPCI Express Specification*.

Within the Backplane Identification and Capability Record is a Peripheral Slot descriptor that requires additional definition and clarification to handle the System Timing Slot and the different names used for slots within PXI Express.

RULE: Bits 2:0 of the Slot Type field of all Peripheral Slot Descriptors within a Backplane Identification and Capability Record of a PXI Express Chassis SHALL have the following definition:

Bits (2:0)
000 = N/A
001 = PXI Express Peripheral Slot
010 = PXI-1 Slot
011 = Hybrid Peripheral Slot
111 = System Timing Slot

4.8 SMBus Address Reservation

The SMBus allows backplane identification to be possible in PXI Express systems. It also allows for suppliers to implement Chassis-specific Functions without needing a PCI Express interface. The SMBus may connect to other devices on System Modules, so it is important that these other devices do not conflict with the Backplane Identification and Capability Record EPROM and any Chassis-specific Functions. This section sets the requirements for SMBus addressing for any Chassis-specific Functions and CompactPCI Express sets addressing requirements for the Backplane Identification and Capability Record EPROM.

Peripheral Module use of SMBus is also possible. To prevent addressing conflicts between Peripheral Modules and other devices on the SMBus, Peripheral Module SMBus devices are required to support the Address Resolution Protocol to have their address assigned.

PERMISSION: System Modules MAY connect devices related to System Module functionality to the SMBus.

OBSERVATION: The CompactPCI Express specification reserves SMBus address A4h for the Backplane Identification and Capability Record EPROM. This requirement applies to PXI Express as well.

RULE: PXI Express System Modules SMBus devices that connect to the SMBus defined in this specification SHALL NOT use SMBus addresses 58h to 5Ch, C6h to C8h, and A4h.

RULE: Any SMBus devices within a PXI Express Chassis for Chassis-specific Functions other than the Backplane Identification and Capability Record EPROM SHALL use addresses 58h to 5Ch.

OBSERVATION: The SMBus addresses specified are 8-bit addresses where the least significant bit represents read or write. This implies that for every even address, an odd address is reserved as well. For example, A4h is the SMBus address to write to the Backplane Identification and Capability Record EPROM, and A5h is the address to read from the Backplane Identification and Capability Record EPROM.

RULE: PXI Express Peripheral Modules that connect devices to the SMBus SHALL implement the Address Resolution Protocol (ARP) defined in the SMBus 2.0 Specification for setting their SMBus addresses of the devices.

4.9 Electrical Guidelines for 6U

In an effort to make efficient use of 3U PXI Express Modules in 6U PXI Express Chassis, the *PXI Express Hardware Specification* defines a 6U Slot that allows 3U Modules to be stacked within. This allows two 3U Modules to be used in 1 6U Slot. These systems have additional connectors in slots that support stacking 3U Modules. This section also covers the electrical rules associated with 6U PXI Express Chassis that support this feature and defines a 6U System Timing Module that can support the differential triggers for 3U Modules that are stacked in a 6U Slot.

4.9.1 6U Chassis that Support Stacking 3U Modules

RULE: 6U PXI Express Chassis that support stacking 3U Modules SHALL route the signals for the upper and lower 3U Slots according to the type of 3U Slots being implemented within the 6U Slot (System, Hybrid, PXI Express Peripheral, PXI-1 or System Timing Slot).

RULE: If a PXI Express 6U Chassis that supports stacking 3U Modules cannot provide enough star triggers or differential triggers to support all slots via the lower 3U Slot within the System Timing Slot, the PXI Express 6U Chassis SHALL support stacking 3U System Timing Modules in the System Timing Slot.

RULE: 6U PXI Express Chassis that support stacking 3U Modules SHALL implement a PXI Express Peripheral Slot or System Timing Slot only in the upper 3U Slot of a 6U System Timing Slot.

RULE: The PCI Express or PCI interfaces needed for the upper 3U Slots of PXI Express 6U Chassis that support stacking 3U Modules SHALL be provided by the backplane and SHALL NOT be provided by the System Controller Module.

OBSERVATION: The preceding rule allows most 6U CompactPCI Express System Modules to work in 6U PXI Express Chassis that support stacking 3U Modules.

4.10 Connector Pin Assignments

4.10.1 PXI Express Peripheral Slots and Modules

RULE: PXI Express Peripheral Slots and PXI Express Peripheral Modules SHALL use the pin assignments in Table 4-9.

Table 4-9. PXI Express Peripheral Slot and Module Pin Assignments

Pin	Z	A	B	C	D	E	F	XP4 / XJ4 Connector
1	GND	GA4	GA3	GA2	GA1	GA0	GND	
2	GND	5Vaux	GND	SYSEN#	WAKE#	ALERT#	GND	
3	GND	12V	12V	GND	GND	GND	GND	
4	GND	GND	GND	3.3V	3.3V	3.3V	GND	
5	GND	PXI_TRIG3	PXI_TRIG4	PXI_TRIG5	GND	PXI_TRIG6	GND	
6	GND	PXI_TRIG2	GND	ATNLED	PXI_STAR	PXI_CLK10	GND	
7	GND	PXI_TRIG1	PXI_TRIG0	ATNSW#	GND	PXI_TRIG7	GND	
8	GND	RSV	GND	RSV	PXI_LBL6	PXI_LBR6	GND	

Pin	A	B	ab	C	D	cd	E	F	ef	XP3 / XJ3 Connector
1	PXIe_CLK100+	PXIe_CLK100-	GND	PXIe_SYNC100+	PXIe_SYNC100-	GND	PXIe_DSTARC+	PXIe_DSTARC-	GND	
2	PRSNT#	PWREN#	GND	PXIe_DSTARB+	PXIe_DSTARB-	GND	PXIe_DSTARA+	PXIe_DSTARA-	GND	
3	SMBDAT	SMBCLK	GND	RSV	RSV	GND	RSV	RSV	GND	
4	MPWRGD	PERST#	GND	RSV	RSV	GND	1RefClk+	1RefClk-	GND	
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	1PETp1	1PETn1	GND	
6	1PETp2	1PETn2	GND	1PERp2	1PERn2	GND	1PERp1	1PERn1	GND	
7	1PETp3	1PETn3	GND	1PERp3	1PERn3	GND	1PETp4	1PETn4	GND	
8	1PETp5	1PETn5	GND	1PERp5	1PERn5	GND	1PERp4	1PERn4	GND	
9	1PETp6	1PETn6	GND	1PERp6	1PERn6	GND	1PETp7	1PETn7	GND	
10	RSV	RSV	GND	RSV	RSV	GND	1PERp7	1PERn7	GND	

4.10.2 PXI Express System Slot and Modules

Two backplane routing schemes are allowed for the System Slot within the CompactPCI Express Specification. The 4 Link configuration maximizes the number of Links from the System Slot to Peripheral Slots, to Switches, to a Switch Slot, or PCI Express to PCI Bridges. However, the highest Lane count for each of the 4 Links is 4 lanes per Link. The 2 Link configuration assumes there are 2 Links coming from the System Board, where one of the Links can be up to eight lanes and the other Link can be up to 16 lanes.

4.10.2.1 4 Link Configuration

RULE: PXI System Slots routed for the 4 Link Configuration SHALL use the pin assignments in Table 4-10.

RULE: PXI System Modules SHALL follow the pin assignments in Table 4-10 to support 4 Link operation.

Table 4-10. Pin Assignments for 4 Link Operation

Pin	Z	A	B	C	D	E	F	
1	GND	GA4	GA3	GA2	GA1	GA0	GND	XP4/ XJ4 Connector
2	GND	5Vaux	GND	SYSEN#	WAKE#	ALERT#	GND	
3	GND	RSV	RSV	RSV	RSV	RSV	GND	
4	GND	RSV	RSV	RSV	RSV	RSV	GND	
5	GND	PXI_TRIG3	PXI_TRIG4	PXI_TRIG5	GND	PXI_TRIG6	GND	
6	GND	PXI_TRIG2	GND	RSV	PXI_STAR	PXI_CLK10	GND	
7	GND	PXI_TRIG1	PXI_TRIG0	RSV	GND	PXI_TRIG7	GND	
8	GND	RSV	GND	RSV	RSV	PXI_LBR6	GND	

Pin	A	B	ab	C	D	cd	E	F	ef	
1	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND	XP3 / XJ3 Connector
2	RSV	RSV	GND	PWR_OK	PS_ON#	GND	LINKCAP	PWRBTN#	GND	
3	SMBDAT	SMBCLK	GND	4RefClk+	4RefClk-	GND	2RefClk+	2RefClk-	GND	
4	RSV	PERST#	GND	3RefClk+	3RefClk-	GND	1RefClk+	1RefClk-	GND	
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	1PETp1	1PETn1	GND	
6	1PETp2	1PETn2	GND	1PERp2	1PERn2	GND	1PERp1	1PERn1	GND	
7	1PETp3	1PETn3	GND	1PERp3	1PERn3	GND	2PETp0	2PETn0	GND	
8	2PETp1	2PETn1	GND	2PERp1	2PERn1	GND	2PERp0	2PERn0	GND	
9	2PETp2	2PETn2	GND	2PERp2	2PERn2	GND	2PETp3	2PETn3	GND	
10	3PETp0	3PETn0	GND	3PERp0	3PERn0	GND	2PERp3	2PERn3	GND	

Pin	A	B	ab	C	D	cd	E	F	ef	
1	3PETp1	3PETn1	GND	3PERp1	3PERn1	GND	3PETp2	3PETn2	GND	XP2 / XJ2 Connector
2	3PETp3	3PETn3	GND	3PERp3	3PERn3	GND	3PERp2	3PERn2	GND	
3	4PETp0	4PETn0	GND	4PERp0	4PERn0	GND	4PETp1	4PETn1	GND	
4	4PETp2	4PETn2	GND	4PERp2	4PERn2	GND	4PERp1	4PERn1	GND	
5	4PETp3	4PETn3	GND	4PERp3	4PERn3	GND	RSV	RSV	GND	
6	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND	
7	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND	
8	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND	
9	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND	
10	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND	

Pin		
G	GND	XP1 / XJ1 Connector
F	12V	
E	12V	
D	GND	
C	5V	
B	3.3V	
A	GND	

4.10.2.2 2 Link Configuration

RULE: System Modules that can combine the four smaller Links into two larger Links SHALL follow the pin assignments in Table 4-11 when in 2 Link operation.

RULE: PXI System Slots routed for the 2 Link Configuration SHALL use the pin assignments in Table 4-11.

Table 4-11. Pin Assignments for 2 Link Operation

Pin	Z	A	B	C	D	E	F
1	GND	GA4	GA3	GA2	GA1	GA0	GND
2	GND	5Vaux	GND	SYSEN#	WAKE#	ALERT#	GND
3	GND	RSV	RSV	RSV	RSV	RSV	GND
4	GND	RSV	RSV	RSV	RSV	RSV	GND
5	GND	PXI_TRIG3	PXI_TRIG4	PXI_TRIG5	GND	PXI_TRIG6	GND
6	GND	PXI_TRIG2	GND	RSV	PXI_STAR	PXI_CLK10	GND
7	GND	PXI_TRIG1	PXI_TRIG0	RSV	GND	PXI_TRIG7	GND
8	GND	RSV	GND	RSV	RSV	PXI_LBR6	GND

XP4 / XJ4 Connector

Pin	A	B	ab	C	D	cd	E	F	ef
1	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND
2	RSV	RSV	GND	PWR_OK	PS_ON#	GND	LINKCAP	PWRBTN#	GND
3	SMBDAT	SMBCLK	GND	RSVD	RSVD	GND	RSVD	RSVD	GND
4	RSV	PERST#	GND	2RefClk+	2RefClk-	GND	1RefClk+	1RefClk-	GND
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	1PETp1	1PETn1	GND
6	1PETp2	1PETn2	GND	1PERp2	1PERn2	GND	1PERp1	1PERn1	GND
7	1PETp3	1PETn3	GND	1PERp3	1PERn3	GND	1PETp4	1PETn4	GND
8	1PETp5	1PETn5	GND	1PERp5	1PERn5	GND	1PERp4	1PERn4	GND
9	1PETp6	1PETn6	GND	1PERp6	1PERn6	GND	1PETp7	1PETn7	GND
10	2PETp0	2PETn0	GND	2PERp0	2PERn0	GND	1PERp7	1PERn7	GND

XP3 / XJ3 Connector

Pin	A	B	ab	C	D	cd	E	F	ef
1	2PETp1	2PETn1	GND	2PERp1	2PERn1	GND	2PETp2	2PETn2	GND
2	2PETp3	2PETn3	GND	2PERp3	2PERn3	GND	2PERp2	2PERn2	GND
3	2PETp4	2PETn4	GND	2PERp4	2PERn4	GND	2PETp5	2PETn5	GND
4	2PETp6	2PETn6	GND	2PERp6	2PERn6	GND	2PERp5	2PERn5	GND
5	2PETp7	2PETn7	GND	2PERp7	2PERn7	GND	2PETp8	2PETn8	GND
6	2PETp9	2PETn9	GND	2PERp9	2PERn9	GND	2PERp8	2PERn8	GND
7	2PETp10	2PETn10	GND	2PERp10	2PERn10	GND	2PETp11	2PETn11	GND
8	2PETp12	2PETn12	GND	2PERp12	2PERn12	GND	2PERp11	2PERn11	GND
9	2PETp13	2PETn13	GND	2PERp13	2PERn13	GND	2PETp14	2PETn14	GND
10	2PETp15	2PETn15	GND	2PERp15	2PERn15	GND	2PERp14	2PERn14	GND

XP2 / XJ2 Connector

Pin	
G	GND
F	12V
E	12V
D	GND
C	5V
B	3.3V
A	GND

XP1 / XJ1 Connector

4.10.3 PXI Express Hybrid Peripheral Slot

RULE: PXI Express Hybrid Peripheral Slots SHALL use the pin assignments in Table 4-12.

Table 4-12. Hybrid Peripheral Slot Pin Assignments

Pin	Z	A	B	C	D	E	F	
1	GND	GA4	GA3	GA2	GA1	GA0	GND	XP4 / XJ4 Connector
2	GND	5Vaux	GND	SYSEN#	WAKE#	ALERT#	GND	
3	GND	12V	12V	GND	GND	GND	GND	
4	GND	GND	GND	3.3V	3.3V	3.3V	GND	
5	GND	PXI_TRIG3	PXI_TRIG4	PXI_TRIG5	GND	PXI_TRIG6	GND	
6	GND	PXI_TRIG2	GND	ATNLED	PXI_STAR	PXI_CLK10	GND	
7	GND	PXI_TRIG1	PXI_TRIG0	ATNSW#	GND	PXI_TRIG7	GND	
8	GND	RSV	GND	RSV	PXI_LBL6	PXI_LBR6	GND	

Pin	A	B	ab	C	D	cd	E	F	ef	
1	PXIe_CLK100+	PXIe_CLK100-	GND	PXIe_SYNC100+	PXIe_SYNC100-	GND	PXIe_DSTARC+	PXIe_DSTARC-	GND	XP3 / XJ3 Connector
2	PRSNT#	PWREN#	GND	PXIe_DSTARB+	PXIe_DSTARB-	GND	PXIe_DSTARA+	PXIe_DSTARA-	GND	
3	SMBDAT	SMBCLK	GND	RSV	RSV	GND	RSV	RSV	GND	
4	MPWRGD	PERST#	GND	RSV	RSV	GND	1RefClk+	1RefClk-	GND	
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	1PETp1	1PETn1	GND	
6	1PETp2	1PETn2	GND	1PERp2	1PERn2	GND	1PERp1	1PERn1	GND	
7	1PETp3	1PETn3	GND	1PERp3	1PERn3	GND	1PETp4	1PETn4	GND	
8	1PETp5	1PETn5	GND	1PERp5	1PERn5	GND	1PERp4	1PERn4	GND	
9	1PETp6	1PETn6	GND	1PERp6	1PERn6	GND	1PETp7	1PETn7	GND	
10	RSV	RSV	GND	RSV	RSV	GND	1PERp7	1PERn7	GND	

Pin	Z	A	B	C	D	E	F	
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND	P1 / J1 Connector
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND	
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND	
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND	
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND	
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND	
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND	
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND	
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND	
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND	
15	GND	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND	
12–14	Key Area							
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND	
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND	
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND	
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND	
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND	
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND	
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND	
4	GND	IPMB_PWR	HEALTHY#	V(I/O)	INTP	INTS	GND	
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND	
2	GND	TCK	5V	TMS	TDO	TDI	GND	
1	GND	5V	-12V	TRST#	+12V	5V	GND	

4.10.4 PXI-1 Slot

RULE: PXI-1 Slots SHALL follow the pin assignments defined in the *PXI Hardware Specification*.

4.10.5 System Timing Slot

RULE: System Timing Modules and System Timing Slots SHALL use the pinouts in Table 4-13.

Table 4-13. PXI Express System Timing Slot/Module Pinout

Pin	Z	A	B	C	D	E	F	
1	GND	GA4	GA3	GA2	GA1	GA0	GND	XP4/XJ4 Connector
2	GND	5Vaux	GND	SYSEN#	WAKE#	ALERT#	GND	
3	GND	12V	12V	GND	GND	GND	GND	
4	GND	GND	GND	3.3V	3.3V	3.3V	GND	
5	GND	PXI_TRIG3	PXI_TRIG4	PXI_TRIG5	GND	PXI_TRIG6	GND	
6	GND	PXI_TRIG2	GND	ATNLED	PXI_CLK10_IN	PXI_CLK10	GND	
7	GND	PXI_TRIG1	PXI_TRIG0	ATNSW#	GND	PXI_TRIG7	GND	
8	GND	PXIe_SYNC_CTRL	GND	RSV	PXI_LBL6	PXI_LBR6	GND	

Pin	A	B	ab	C	D	cd	E	F	ef	
1	PXIe_CLK100+	PXIe_CLK100-	GND	PXIe_SYNC100+	PXIe_SYNC100-	GND	PXIe_DSTARC+	PXIe_DSTARC-	GND	XP3/XJ3 Connector
2	PRSNT#*	PWREN#*	GND	PXIe_DSTARB+	PXIe_DSTARB-	GND	PXIe_DSTARA+	PXIe_DSTARA-	GND	
3	SMBDAT	SMBCLK	GND	RSV	RSV	GND	RSV	RSV	GND	
4	MPWRGD*	PERST#	GND	RSV	RSV	GND	1RefClk+	1RefClk-	GND	
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	1PETp1	1PETn1	GND	
6	1PETp2	1PETn2	GND	1PERp2	1PERn2	GND	1PERp1	1PERn1	GND	
7	1PETp3	1PETn3	GND	1PERp3	1PERn3	GND	1PETp4	1PETn4	GND	
8	1PETp5	1PETn5	GND	1PERp5	1PERn5	GND	1PERp4	1PERn4	GND	
9	1PETp6	1PETn6	GND	1PERp6	1PERn6	GND	1PETp7	1PETn7	GND	
10	RSV	RSV	GND	RSV	RSV	GND	1PERp7	1PERn7	GND	

Pin	A	B	ab	C	D	cd	E	F	ef	
1	PXIe_DSTARC0+	PXIe_DSTARC0-	GND	PXIe_DSTARC8+	PXIe_DSTARC8-	GND	PXIe_DSTARB8+	PXIe_DSTARB8-	GND	TP2/TJ2 Connector
2	PXIe_DSTARA0+	PXIe_DSTARA0-	GND	PXIe_DSTARC9+	PXIe_DSTARC9-	GND	PXIe_DSTARA8+	PXIe_DSTARA8-	GND	
3	PXIe_DSTARB0+	PXIe_DSTARB0-	GND	PXIe_DSTARC1+	PXIe_DSTARC1-	GND	PXIe_DSTARA9+	PXIe_DSTARA9-	GND	
4	PXIe_DSTARB1+	PXIe_DSTARB1-	GND	PXI_STAR0	PXI_STAR1	GND	PXIe_DSTARB9+	PXIe_DSTARB9-	GND	
5	PXIe_DSTARA1+	PXIe_DSTARA1-	GND	PXI_STAR2	PXI_STAR3	GND	PXIe_DSTARC10+	PXIe_DSTARC10-	GND	
6	PXIe_DSTARC2+	PXIe_DSTARC2-	GND	PXI_STAR4	PXI_STAR5	GND	PXIe_DSTARA10+	PXIe_DSTARA10-	GND	
7	PXIe_DSTARB2+	PXIe_DSTARB2-	GND	PXI_STAR6	PXI_STAR7	GND	PXIe_DSTARB10+	PXIe_DSTARB10-	GND	
8	PXIe_DSTARA2+	PXIe_DSTARA2-	GND	PXI_STAR8	PXI_STAR9	GND	PXIe_DSTARC11+	PXIe_DSTARC11-	GND	
9	PXIe_DSTARC3+	PXIe_DSTARC3-	GND	PXI_STAR10	PXI_STAR11	GND	PXIe_DSTARA11+	PXIe_DSTARA11-	GND	
10	PXIe_DSTARB3+	PXIe_DSTARB3-	GND	PXIe_DSTARC16+	PXIe_DSTARC16-	GND	PXIe_DSTARB11+	PXIe_DSTARB11-	GND	

Pin	A	B	ab	C	D	cd	E	F	ef	
1	PXIe_DSTARA3+	PXIe_DSTARA3-	GND	PXIe_DSTARC7+	PXIe_DSTARC7-	GND	PXIe_DSTARC12+	PXIe_DSTARC12-	GND	TP1/TJ1 Connector
2	PXIe_DSTARC4+	PXIe_DSTARC4-	GND	PXI_STAR12	PXI_STAR13	GND	PXIe_DSTARA12+	PXIe_DSTARA12-	GND	
3	PXIe_DSTARB4+	PXIe_DSTARB4-	GND	PXIe_DSTARA16+	PXIe_DSTARA16-	GND	PXIe_DSTARB12+	PXIe_DSTARB12-	GND	
4	PXIe_DSTARA4+	PXIe_DSTARA4-	GND	PXIe_DSTARB7+	PXIe_DSTARB7-	GND	PXIe_DSTARC13+	PXIe_DSTARC13-	GND	
5	PXIe_DSTARC5+	PXIe_DSTARC5-	GND	PXI_STAR14	PXI_STAR15	GND	PXIe_DSTARA13+	PXIe_DSTARA13-	GND	
6	PXIe_DSTARB5+	PXIe_DSTARB5-	GND	PXIe_DSTARB16+	PXIe_DSTARB16-	GND	PXIe_DSTARB13+	PXIe_DSTARB13-	GND	
7	PXIe_DSTARA5+	PXIe_DSTARA5-	GND	PXIe_DSTARA7+	PXIe_DSTARA7-	GND	PXIe_DSTARC14+	PXIe_DSTARC14-	GND	
8	PXIe_DSTARC6+	PXIe_DSTARC6-	GND	PXI_STAR16	RSV	GND	PXIe_DSTARA14+	PXIe_DSTARA14-	GND	
9	PXIe_DSTARB6+	PXIe_DSTARB6-	GND	PXIe_DSTARC15+	PXIe_DSTARC15-	GND	PXIe_DSTARB14+	PXIe_DSTARB14-	GND	
10	PXIe_DSTARA6+	PXIe_DSTARA6-	GND	PXIe_DSTARB15+	PXe_DSTARB15-	GND	PXIe_DSTARA15+	PXIe_DSTARA15-	GND	

4.11 POWER

The power requirements for PXI Express Chassis and Modules include all requirements defined in the *CompactPCI Express Specification*, as well as additional rules that set minimum requirements for power provided by Chassis. These additional rules enhance the interoperability between Modules and Chassis.

4.11.1 Power Requirements from CompactPCI Express

RULE: PXI Express Chassis and Modules SHALL meet all the rules relating to power defined within the CompactPCI Express specification. These rules include but are not limited to the following:

- Voltage rails
- Current capacity of the power pins for a slot
- Regulation
- Ripple and noise
- Backplane power decoupling
- Power rail timing
- Power supply signals to and from the System Module and the associated timing requirements

4.11.2 Chassis Requirements

Minimum power supply requirements are specified to ensure that Module designers can design Modules knowing that they will operate in any PXI Express Chassis regardless of the number of slots or form factor.

4.11.2.1 Minimum Required Continuous Current

RULE: The power supply in a PXI Express Chassis SHALL provide at least the required amounts of continuous current and total power per slot specified in Table 4-14.

Table 4-14. PXI Express Chassis Minimum Required Continuous Current

	5 V	3.3 V	+12 V	-12 V	5 V_{AUX}	Total Power	Notes
System Controller Slot with 2 or More Expansion Slots	9 A	9 A	11 A	N/A	1 A	140 W	1, 2
System Controller Slot with 1 Expansion Slot	2 A	6 A	4 A	N/A	1 A	60 W	1
System Controller Slot with no Expansion Slots	1 A	3 A	2 A	N/A	1 A	30 W	1
PXI Express Peripheral Slot / System Timing Slot	N/A	3 A	2 A	N/A	0 A	30 W	1, 3
Hybrid Slot	2 A	3 A	2 A	0.25 A	0 A	30 W	1, 3, 4
PXI-1 Peripheral Slot	2 A	2 A	0.5 A	0.25 A	N/A	25.6 W	1

Notes:

1. The PXI Express Chassis is required to provide only the combined power specified in the Total Power column.
2. The PXI Express Chassis is required to provide only a total of 61.5 W combined power on 3.3 V and 5 V a System Controller Slot with two or more expansion slots.
3. There SHALL be 0.5 A of $5V_{AUX}$ available for all PXI Express Peripheral Modules to share.
4. A Hybrid Slot SHALL provide the continuous current required for a PXI Express Peripheral Module OR a PXI-1 Peripheral Module (not both at the same time).

OBSERVATION: The minimum current for each voltage rail provided by a power supply in a PXI Express Chassis with X PXI Express Peripheral Slots, Y Hybrid Slots, and Z PXI-1 Peripheral Slots can be determined by the following formulas:

+12 V: $11\ A + (X + Y) \times 2\ A + Z \times 0.5\ A$

3.3 V: $9\ A + (X + Y) \times 3\ A + Z \times 2\ A$

5 V: $9\ A + (Y + Z) \times 2\ A$

-12 V: $(Y + Z) \times 0.25\ A$

5 V_{AUX}: 1.5 A if $(X + Y) > 0$; else 1 A

For an 8-slot Chassis with one PXI Express System Timing Slot, two Hybrid Slots, and four PXI-1 Slots, the minimum current for each voltage rail for the entire Chassis would be as follows:

+12 V: $11\ A + (1 + 2) \times 2\ A + 4 \times 0.5\ A = 11\ A + 6\ A + 2\ A = 19\ A$

3.3 V: $9\ A + (1 + 2) \times 3\ A + 4 \times 2\ A = 9\ A + 9\ A + 8\ A = 26\ A$

5 V: $9\ A + (2 + 4) \times 2\ A = 9\ A + 12\ A = 21\ A$

-12 V: $(2 + 4) \times 0.25\ A = 1.5\ A$

5 V_{AUX}: 1.5 A

For a 14-slot Chassis with one PXI Express System Timing Slot, two PXI Express Peripheral Slots, six Hybrid Slots, and four PXI-1 Slots, the minimum current for each voltage rail for the entire Chassis would be as follows:

+12 V: $11\ A + (3 + 6) \times 2\ A + 4 \times 0.5\ A = 11\ A + 18\ A + 2\ A = 31\ A$

3.3 V: $9\ A + (3 + 6) \times 3\ A + 4 \times 2\ A = 9\ A + 27\ A + 8\ A = 44\ A$

5 V: $9\ A + (6 + 4) \times 2\ A = 9\ A + 20\ A = 29\ A$

-12 V: $(6 + 4) \times 0.25\ A = 2.5\ A$

5 V_{AUX}: 1.5 A

OBSERVATION: The minimum power provided by a power supply in a PXI Express Chassis with X PXI Express Peripheral Slots, Y Hybrid Slots, and Z PXI-1 Slots can be determined by the following formula:

$140\ W + (X + Y) \times 30\ W + Z \times 25.6\ W$

PERMISSION: PXI Express Chassis MAY provide additional current beyond what is required in Table 4-14.

OBSERVATION: Each generation of processors requires more power than the previous generation. Providing copious amounts of power and cooling to the System Slot of a Chassis can extend the product applicability in the future.

RULE: A PXI Express Chassis SHALL have its DC current output capability documented and available to the end users.

RULE: A PXI Express Chassis backplane and connectors SHALL be capable of transferring the amount of current specified in Table 4-15 to each slot.

RULE: The backplane and connectors SHALL be capable of receiving as much return current as they are capable of delivering.

Table 4-15. PXI Express Backplane Continuous Current Capability

	5 V	V(I/O)	3.3 V	+12 V	-12 V	5 V_{AUX}	Notes
PXI Express System Controller Slot	15 A	0 A	15 A	30 A	0 A	1 A	1
PXI Express Peripheral Slot	0 A	0 A	3 A	2 A	0 A	1 A	
Hybrid Slot	6 A	5 A	6 A	2 A	1 A	1 A	
PXI-1 Peripheral Slot	6 A	11 A	6 A	1 A	1 A	0 A	

Notes:

1. Maximum combined current from 12 V, 3.3 V, and 5 V on the PXI Express System Controller Slot is 45 A.

4.11.2.2 Low-Power Chassis Power Supply Specifications

A Chassis designed for portable application or one with a DC power input may be constrained by the battery and operating hours. This may make meeting the minimum power requirements listed in Table 4-14 impractical, but minimum power requirements for this class of Chassis are still important for interoperability with Modules. The minimum power requirements for low-power Chassis are set to allow at least one PXI Express System Module that requires no expansion slots and two PXI Express Peripheral Modules to work in the Chassis, regardless or 3U/6U or the number of slots available.

PERMISSION: A low-power PXI Express Chassis MAY provide less power than is required in Table 4-14.

RULE: A low-power PXI Express Chassis with less power than is required in Table 4-14 SHALL provide at least the minimum output current necessary for a PXI Express System Module that requires no expansion slots and any two Peripheral Slots (PXI Express, Hybrid or PXI-1) that are in the Chassis.

RULE: PXI Express Chassis having less power than is required in Table 4-14 and meeting the power requirement for a low-power PXI Express Chassis SHALL have the text LOW POWER clearly visible with a character height of at least 4 mm on the front of the Chassis, as shown in Figure 4-12. Logo artwork can be obtained from the PXI Systems Alliance.

Figure 4-12. Text Required for Low-Power Chassis

4.11.3 Module Requirements

The purpose of this section is to provide rules and recommendations for interoperability between the PXI Express System Controller and Peripheral Modules.

4.11.3.1 Maximum Continuous Current Draw

PERMISSION: A PXI Express System Controller or Peripheral Module MAY draw more continuous current than the Chassis is required to provide in Table 4-14.

RULE: A PXI Express System Controller or Peripheral SHALL NOT draw more continuous current from the voltage rails of a slot than the maximum continuous current capabilities specified in Table 4-15.

RULE: A PXI Express System Controller or Peripheral Module SHALL publish its maximum continuous current requirements to the end user.

4.12 Chassis Grounding

Reference the *PXI Hardware Specification* for Chassis grounding requirements.

5. Regulatory Requirements

The following standards assure uniform performance and international portability of PXI systems and Modules. All regulatory compliance information must be clearly documented for the user. Subsequently issued standards or amendments to these standards SHALL apply.

5.1 Requirements for EMC

RULE: Testing SHALL be performed for all PXI Express Modules and Chassis, either by the manufacturer or a competent laboratory, marked accordingly, and documented showing compliance to the following electromagnetic compatibility (EMC) standard(s). The latest released or accepted standard should be used. A competent laboratory should be qualified by a recognized accreditation body for EMC.

IEC 61326-1, *Electrical Equipment for Measurement, Control, and Laboratory Use—EMC Requirements—Part I, General Requirements*:

- Localized EMC standards may be substituted if sale and use are restricted accordingly.
- Use current edition of EN 55011, Group 1, Class A or Class B Limits, at 10 m for radiated emissions testing.

5.2 Requirements for Electrical Safety

RULE: Safety testing SHALL be performed for all PXI Express Modules and Chassis, either by an accredited safety organization[1] and marked accordingly (preferred), or tested by a qualified manufacturer, and documented showing compliance to the following electrical safety standard(s). Strictly safety extra low-voltage (SELV) devices do not need formal agency testing, though the basic requirements still apply, such as material flammability, DC power outputs fused or limited, and so on.

IEC 61010-1, Second Edition (2001), *Safety Requirements for Electrical Equipment for Measurement, Control, and Laboratory use—Part 1, General Requirements*:

- IEC 60950 and amendments are acceptable for applications restricted to the office use only.
- Localized safety standards may be substituted if sale and use are restricted accordingly, and laws allow. [2]
- All relevant safety laws and standards must be met for country(s) of use.

5.3 Additional Requirements for Chassis

RULE: A PXI Express Chassis SHALL be qualified for electrical safety as listed previously. Manufacturer claims of safety compliance are not sufficient without independent certification and regular inspection by a competent safety organization.

RULE: PXI Express Chassis manufacturers, or a designated party, SHALL demonstrate EMC compliance with a commonly available Controller. A reasonably common processor speed is sufficient for this test. The complete Controller system, including hard drive, floppy drive, serial, parallel, keyboard, mouse, and video ports (as offered with the Controller) will be exercised with typical Peripherals. Filling remaining slots, if any, is not required.

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[1] Examples of accredited safety organizations are NRTLs in the U.S. and Notified Bodies in Europe.

[2] The use of localized EMC or safety standards must be clearly documented for the benefit of the user. The standards used may include standards in force during legally allowed transitional periods of new standards or amendments. Currently, manufacturer declarations must list all standards used for declaring compliance and conveniently meet this requirement when the declarations are included with the user documentation.

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6. *PXI Express Software Specification* Compliance

RULE: PXI Express Modules, Chassis, and systems SHALL comply with the rules defined in the PXI-6: *PXI Express Software Specification* maintained by the PXI Systems Alliance.

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